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(54) **Active matrix light valve device.**

(57) The present invention provides an improved structure of highly fine light valve device.

On a quartz glass substrate 1, a monocrystalline silicon thin film layer 2 is bonded thereto. Accordingly, the display elements and ancillary circuits can also be formed on the same substrate. Such circuits include an X driving circuit 6 and a Y driving circuit 8 integrated by a very large scale integration process, driving electrodes 5 of a matrix type for conducting signals outputted from the X and Y driving circuits 6, 8, a transistor 9 and a display pixel lectrod 10 arrang d at a cross s ction of the driving lectrodes 5, a control circuit 4 for supplying timing signals to the X and Y driving circuits 6, 8, a display data generating circuit 3 for generating display data in order to display an image, and further a light source element driving circuit 19 for driving a light source element.

The present invention thus provides an improved enforced structure of the light valve device having high reliability which is convenient to use, of a very compact size, of high density and high accuracy.

The device can be used to provide stereoscopic images when the elements driv n by th X driving circuits are latticed so that alt rnat lements relat to the input imag s from "on ey " and the other el m nts from the "other ey ".

EP 0 593 266 A2

An image projector is also disclosed which includes a light valve cell having a high integration density in order to achieve highly accurate images. Moreover, the cell is provided with means for cooling so as to effectively obviate temperature rises.

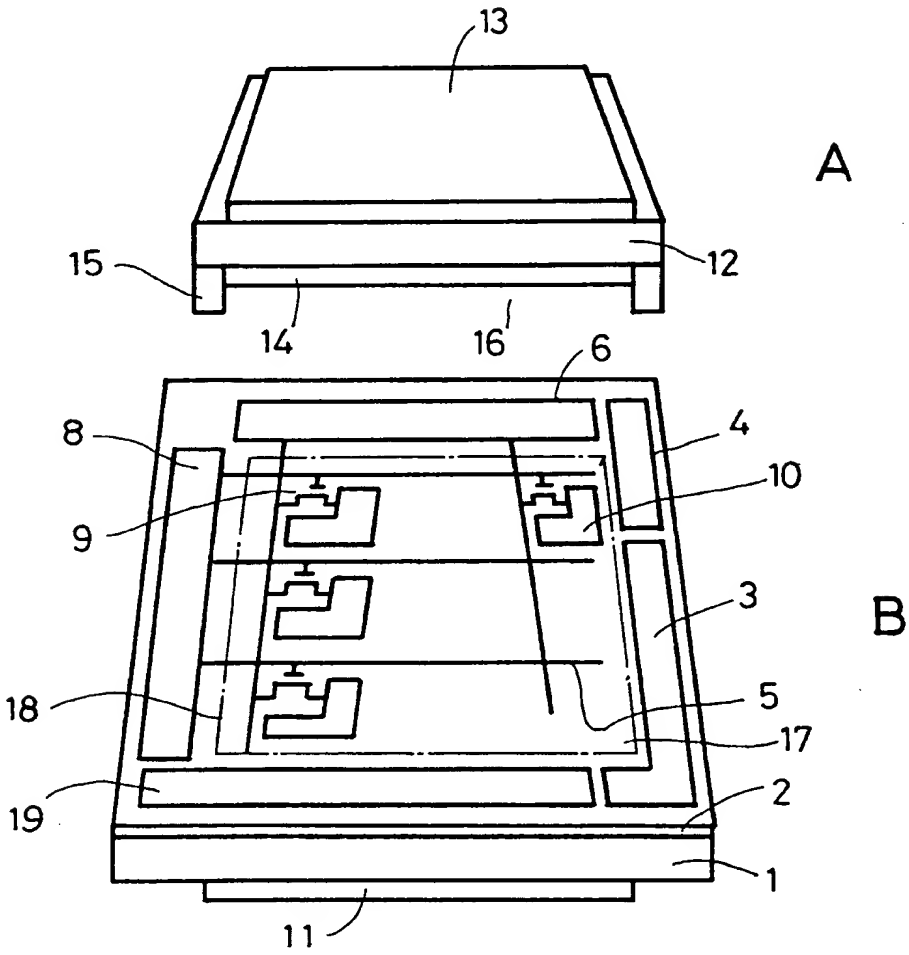


FIG. 1

The present invention relates to active matrix type light valve devices, stereoscopic image display devices and image projectors. The active matrix type light valve devices use monocrystalline semiconductor layers as an active region. The stereoscopic image display devices are capable of observing images from the light valve devices provided on both eyes to obtain stereoscopic vision. The image projectors are composed of a light source section, the light valve device, and a projection optical system.

Conventionally, compact type light valve devices have been used to display images as, for example, view finders of 8mm video cameras. The devices are made by depositing polycrystal or amorphous silicon thin films on transparent electrically insulating substrates by vapour depositing or vapour phase epitaxy to form an individual-pixel switching element group and an X-Y electrode driving circuit group for driving each such switching element group by the thin film transistors.

The general configuration of such a conventional active matrix type liquid crystal display device is described with reference to figure 40. In the image display device of this kind, one quartz glass substrate 1001 and the other glass substrate 1012 are oppositely arranged to each other and a liquid crystal layer 1016 is sealed between the substrates. On a main surface of the quartz glass substrate 1001 is formed a film of a silicon polycrystal semiconductor layer 1002P, which constitutes an active region. A pixel array section 1017 and a peripheral circuit section are integrally formed on an inside surface of the quartz glass substrate 1001. The peripheral circuit section includes an X axis driving circuit 1006 and a Y driving circuit 1008. Matrix driving electrodes 1005 are formed on the pixel array section 1017 in the X axis and Y axis direction so as to orthogonally intersect, and pixel electrodes 1010 are formed on intersecting points thereof. A number of switching elements 1009 are arranged each corresponding to a respective individual pixel electrode 1010. The switching elements 1009 are composed of thin film transistors (TFT) having the silicon polycrystal semiconductor layer 1002P as an active region. Drain electrodes thereof are connected to the corresponding pixel electrodes 1010 and source electrodes thereof are electrically connected to the corresponding X axis matrix driving electrodes 1005. The gate electrodes thereof are electrically connected to the corresponding Y axis matrix driving electrode 1005.

The Y axis driving circuit 1008 selectively scans the matrix driving electrodes 1005 of the Y axis direction in a linear sequence. The X axis driving circuit 1006 is electrically connected to the matrix driving electrodes 1005 of the X axis direction and feeds display signals to the pixel electrodes 1010 through the selected switching elements 1009.

A polariser 1011 is bonded on an outer surface of the quartz glass substrate 1001. A common electrode 1014 is formed entirely on an inner surface of the other glass substrate 1012. A colour filter with three original colours RGB is simultaneously formed for colour display. A polariser 1013 is bonded on outer surface of the glass substrate 1012.

The substrate 1012 on the upper side is bonded to the quartz glass substrate 1001 on the down side by a seal agent 1015. The seal agent 1015 is arranged along a seal region 1018 shown by dotted lines. The seal region 1018 is provided to embrace the pixel array section 1017, the peripheral circuit section composed of the X driving circuit 1006 and Y driving circuit 1008 are positioned outside the seal region 1018.

The amorphous silicon thin film and polycrystal silicon thin film are easily deposited on the glass substrate by chemical vapour phase epitaxy or like procedures. Thus, they are suitable for producing an active matrix type liquid crystal display device having a relatively large display. The transistor elements formed into the amorphous silicon thin film or the polycrystal silicon thin film are generally of a field effect insulating gate type. The amorphous silicon thin film can be formed at a low temperature equal to or less than 350°C and therefore it is again suitable for a large-area liquid crystal panel. At present, displays included in active matrix type liquid crystal display devices using the amorphous silicon thin film which are commerical manufacture to a size of 7.62 to 25.4 x 10^{-2} m the active matrix type liquid crystal display device using the polycrystal silicon thin film is now produced which includes display of a picture size approximately 5.08 x 10^{-2}m (2 inches) in the market.

Although the conventional active matrix type liquid crystal display device using the amorphous silicon thin film or the polycrystal silicon thin film is suitable for direct-view type display devices using relatively large displays, it is not always suitable for miniaturising the devices and achieving a high density of pixels. Recently, microminiature type display devices or light valve devices with a microminiature structure with high density pixels are now increasingly in strong demand, rather than the direct-view type display device. Such microminiature type light valve device is, for example, used as a primary image forming display of the image projector, and can be applied for the hi-vision projection type television. The application of the technique in producing fine semiconductors provides the microminiature type light valve device having a pixel size in the order of 10 μm and with an entire size of several centimeters.

Some secondary problems arise in using the active matrix type liquid crystal display device as a light valve device of the projector. The drawbacks include damage of its light valve function due to temperature rise. In the projector, the light source intensively lights the transmission type liquid crystal display device to

project the transmitted light forwardly through an enlarged optical system. Such intensiv light from th light source is absorb d in th liquid crystal display device so as to cause temperature rises. Thus, if the temperature exceeds a critical point, the liquid crystal phase itself turns to be liquid and is not liquid crystal any more.

The use of the active matrix type liquid crystal display device as a light valve device provides a further drawback in that there is a relatively low brightness of the projected image. This is because, the pixel image accounts for relatively too small a ratio of space of the entire liquid crystal panel surface to provide a sufficient opening ratio. This prevents brightness of the projected image from increasing because of low utilisation efficiency of the light. In addition, the polariser, which absorbs light, is generally bonded on the liquid crystal panel, and so thereby decreases the amount of transmitted light. Therefore, the use of the liquid crystal panel as a light valve device disadvantageously causes a lower utilisation efficiency of the light.

Conventionally, the light source is used only for lighting the light valve device, and is not intended for other utilisations. The projector requires an intensive light source capable of a large amount of energy radiation. However, most of such energy is lost uselessly. Thus, a problem arises in that it is necessary to provide a large projector power supply.

Using parallax of both eyes has conventionally been proposed to view images stereoscopically. For example, (1) a first proposal is to pick up separately, images for the left eye and right eye using two cameras. The images are projected alternatively on a monitor or a screen by switching from one image to the other. A liquid crystal shutter device is used to turn alternatively ON or OFF the left eye image and the right eye image in synchronisation with the switching period of the projected images. Thus, the left eye watches the image prepared for the left eye and the right eye watches the image prepared for the right eye so to view images stereoscopically. (2) A second proposal is to arrange image display elements separately in front of both eyes to display different images for each of the both eyes. Thus, a method of stereoscopic viewing is provided.

However, the conventional amorphous or polycrystal silicon thin film hardly operates at a high speed because of its lower driving current due to its monocrystalline material. For example, mobility of the amorphous silicon thin film is about 1 cm^2/Vsec and so this obviates any need for a high speed peripheral circuit to be formed on the same substrate. Moreover, it is impossible to form a sub-micron order of transistor elements even by applying the microminiature semiconductor t chnique. When using polycrystal silicon thin film, th crystal particl s ach have a size of approximately s veral μm so as to correspondingly limit the fin planning of the transistor el ments. Accordingly, in th conv ntional compact siz imag display devic s using polycrystal or amorphous silicon thin films, it is extremely difficult to realise an integration density and high speed operation similar to those of the ordinary semiconductor integrated circuit elements.

Transmission type panels, such as view finders, require light source elements. However, the active elements of these driving circuits need to be composed of discrete parts because of the requirements for a high voltage resistance and large driving current. Hence, it is difficult to produce an integrated unit as a display device containing light source elements, which is a problem in realising a compact size and convenience on utilisation.

There are further limitations on the electrical performance, in that it is impossible to assemble both the control circuit for supplying timing signals to the peripheral circuit section, for example the driving circuit, and the driving circuit for the light source elements together on one substrate which is necessary for high speed operation. Also in view of the integration density, the increase in size prevents the other peripheral circuits from being incorporated therein. For this reason, in the present situation, it is impossible to assemble the peripheral circuit section, other than the pixel array section and the driving circuit group thereof on one substrate.

In view of the conventional problems mentioned above, the present invention is directed to providing display elements for a compact size image display device in which the switching elements for selectively supplying electricity to the respective pixels and a highly integrated high speed peripheral circuit are formed on one substrate. The peripheral circuit including a driving circuit capable of driving the light source elements with a high voltage resistance and large current.

The present invention provides an improved reinforced structure of the light valve device with high reliability, high utility convenience, microstructure, high density and high accuracy by integrating the light source elements and the display elements into a unitary structure. In particular, another object is to provide a packaging construction of a light valve device which is of a compact size, solid, easy to handle, reliable and provides light shielding, cooling, and is easy to assemble. Further, another object is to improve the image reproducing quality by preventing attenuation of the display signals. Still another object is to improve very fine images by saving display data transfer speed in the circuits by increasing the number of matrix driving electrode groups correspondingly. In addition, another object is to provide fine and highly accurat display devices suitabl for vi w finders and the like by reducing of the outer siz s of th flat panels.

In th methods of ster oscopic view in th prior art as described abov , m thod (1) has a problem in tiring th eyes du to flickering of the imag , m thod (2) requires display elements using the transparent substrate formed of the pixel array section and the driving circuit on the polycrystal silicon thin film. In view of the electrical performance, it is impossible to assemble both the control circuit for supplying timing signals to the peripheral circuit section (for example, the driving circuit) necessitating the high speed operation, and the driving circuit for the light source elements together on the same substrate. In view of the integration density, the increase in size prevents the other peripheral circuits from being incorporating therein. For this reason, in the present situation, it is impossible to assemble the peripheral circuit section other than the pixel array section and the driving circuit group thereof on one substrate. Hence, the peripheral circuits other than the driving circuits need to be formed with the external circuits. Moreover, image data generated by the external circuits and timing signals, both must be connected by wires and this is inconvenient to handle and operate.

In addition, space is required for disposing of light source elements for irradiating the display elements and the pixel array section of the display elements from the back-side thereof. This causes a problem of providing a construction.

To solve the problems hereinbefore described, the present invention comprises at least a transparent electrically insulating substrate and a semiconductor monocrystalline thin film regulating a peripheral circuit area arranged in at least a part of the substrate surface. A pixel array area is provided adjacent to the peripheral circuit area, a pixel electrode group and a switching element group for selectively supplying electricity to each pixel electrode is also provided. The switching element group is driven by X and Y driving circuits. There are similarly included a control circuit for supplying timing signals to the X and Y driving circuits, a display data generating circuit for generating display data, and a receiving circuit for receiving image data through radio communication. The peripheral circuit and driving circuit switching element groups are integratedly formed, for example, using very large-scale integrated circuit (VLSI) manufacturing technique.

To produce such a compact type image display device, for example, a high quality silicon monocrystalline wafer ordinarily used for forming VLSI, is bonded on the transparent electrically insulating substrate. This wafer is mechanically or chemically abraded to produce a semiconductor thin film on an entire surface of the substrate. The semiconductor monocrystalline thin film is selectively processed by VLSI producing techniqu s to form a first transpar nt substrate. On this first transpar nt substrate is formed switching elem nts, X and Y driving circuits, a control circuit and a light source lement driving circuit for driving light source l ments. N xt, the s cond transpar nt substrat composed of a transpar nt el ctrically insulating substrate is arranged with the common electrode provided in the region opposed to the pixel array group formed on the first transparent substrate. The electro-optic material is sealed into a gap between the first and second substrates to constitute the display elements. Electro-luminescence elements (EL element), fluorescence lamp elements (FL element) and the like as a light source element of the display elements are disposed on the backside of the display elements. This mounting on the inside provides a tightly sealed integral unit structure.

According to one embodiment of the present invention, the display data generating circuit includes a RGB conversion circuit for converting composite video signals into RGB display signals and a synchronous separation circuit for separating synchronising signals from the composite video signals. The control circuit generates the timing signals depending on the synchronising signals. According to another embodiment, the driving circuit section includes two sets of X driving circuits and one set of Y driving circuits. The two sets of X driving circuits are arranged separately upper and lower relative to the pixel array section, and operated parallel to each other in accordance with the predetermined timing signals. On the other hand, the Y driving circuit, control circuit, and display data generating circuit are arranged separately on left and right to the pixel array section. According to another embodiment f the invention, the display data generating circuit includes an A/D converter circuit for converting analogue display signals temporarily into digital display data. The driving circuit section includes a D/A converter circuit for re-converting the digital display data into the analogue display signals. According to still another embodiment the pair of substrates are bonded to each other by a seal region provided along the peripheral portion of the substrates. This seal region is arranged to overlap lively with the peripheral circuit section including the driving circuit section, the control circuit, the display data generating circuit.

The present invention is to provide an improved structure of a light valve device with a microminiature size, high density and high accuracy. Particularly, an object is to provide the mount structure of the light valve device superior in size, solidity, handling, reliability, light shielding, cooling, and assembling and like factors. To achieve such objects, an IC package type monocrystalline semiconductor light valve device has been invented. The light valve device according to the invention has an IC package structure in which light valve cells, connector terminals, and packag memb rs are formed into a unitary shape. Th packag memb rs mbrac the light valv cells to nhanc th m physically, and possess a structured por-

tion for shi lding a window section matching to th pix l array s ction and the peripheral circuit section. Th connector t rminals hav on nd electrically connected to the peripheral circuit section of the light valve cells and the other end protruding from the package member.

The package member may preferably be made of black moulded resin product, otherwise the package member may be formed of ceramic mould product. The window section of the package member is attached in unitary shape with a protecting glass member. According to one embodiment of the present invention, the package member has the same thickness as that of the light valve cell. The package member is provided on its external surface with heat radiating fins, or the window of package member is attached with an infrared ray filter for cutting heat rays. The infrared ray filter is laminated sometimes on the polariser disposed apart from the light valve cell. According to another embodiment, the package member has a through hole to be a flow path of coolant. For a particular embodiment, the package member is provided with a recess portion for detachably holding the light valve cell.

The connector terminals are disposed in parallel with the light valve cell and in a manner of protruding from the lateral end surface of the package member. Otherwise, the connector terminals may preferably be arranged in orthogonal to the light valve cell and in a manner of protruding from the main surface of the package member.

An object of the present invention is to provide a projector light valve device having a high density and high accuracy with a compact size. In addition, an object is to provide a cooling structure effectively suppressing temperature rise of the light valve device. Another object is to improve a lightness of the projecting images. Further, an object is to provide a possibility of effectively utilising light source energy. To achieve the objects, various counter measures are taken as undermentioned. The projector according to the invention includes as a basic constituent element a light source section, a light valve device, and a projection optical system. The light valve device includes a pair of transparent substrates disposed opposingly each other, and an electro-optic material arranged between the substrates. On one transparent substrate, a pixel array section and a peripheral circuit section for driving that section are provided. The other transparent substrate is provided thereon with a counter electrode. As a feature of the present invention, the peripheral circuit section is integratedly formed on the monocrystalline semiconductor layer provided on the one transparent substrate.

Preferably, the pixel array section includes a pixel electrod group arranged in matrix shap and a switching element group for selectively pow r supplying to individual pix l el ctrodes, and at least, one of th transparent substrates includes a light-reflectiv shield film for shi lding individual switching elements from incid nt light. Pr ferably, a solar cell is integrally formed on the semiconductor layer to photoelectrically convert incident light and to directly supply a power supply voltage to the peripheral circuit section. More preferably, the light valve device includes a micro-lens array to converge the incident light and to selectively light the pixel electrode group contained in the pixel array section. The micro-lens array is adhered on one of the transparent substrates through a transparent adhesion layer having a smaller refractive index compared therewith. In addition, the light valve device preferably includes a cooling means, which concretely is composed of a container for containing the light valve device, and provided with an inlet for introducing compressed gas and an outlet for discharging decompressed gas to cool the device by means of adiabatic expansion. Or, the cooling means includes a fan for sending cooling gas to the light valve device. Or, the cooling means is composed of the container for containing the light valve device and a cooling system connected to the container and for supplying cooling gas. The cooling system is provided with an automatic temperature control arrangement. A supply port and a discharge port of the cooling system are provided together on lateral surface of the container.

In the display device as constructed above, a substrate with a double layered structure composed of an insulating substrate and a semiconductor monocrystalline thin film formed thereon is used and the semiconductor monocrystalline thin film layer has the same quality as that of a wafer formed of semiconductor monocrystalline bulk. Accordingly, the VLSI manufacturing technique is used to integrate switching elements, and a driving circuit for driving the pixels and peripheral circuits such as a receiving circuit, at ordinary electric performance with a high density, high withstand voltage, and large current driving. In addition, the display elements and the light source elements are made unitary to produce a display device which constitutes a stereoscopic vision display device for binocular, thus a wireless stereoscopic view image display device of a compact size can be provided.

Further in this construction, a video signal processing function and the like can be added to a flat panel device and is suitable for a view finder and the like of the video cameras. The peripheral circuit employs a digital type, and not the conventional analogue type. Thus, the analogue video signals are converted into the digital display data for data processing or data transfer, thereafter at a final stage, the digital display data is re-converted into the analogue display signals to driv the pixel array s ction, henc an xcell nt imag reproducibility is secured without attenuation of display signal. Th VLSI manufacturing

t chniqu is us d to parallely op rat using th driving circuit as a split structur and to d creas driving frequ ncy, thus, corr spondingly th numb r of matrix driving electrodes can be increased to achieve highly accurate images. Moreover, the peripheral circuit section is disposed on periphery of the pixel array section in the centre and the seal region is arranged so as to overlay the peripheral circuit section, there can be obtained a highly integrated multi-functional compact image display device in which a centre of the display picture is substantially coincident with the centre of the flat panel.

According to the present invention, the light valve cell is constituted using the monocrystalline semiconductor layer to integrate and form the peripheral circuit section and the pixel array section into a unitary shape with a high density, thus a microminiature type highly precise light valve cell can be obtained. The light valve cell, the connector terminals, and the package member are integrally formed to provide an IC package construction. Therefore, as in the ordinary IC device, it is extremely easy to handle and is readily assembled into the circuit substrate and the like. In addition, a high grade of solidity, compact size, and reliability are provided because of mould products, and moreover, a shielding effect and cooling effect are given depending on requirement to be suitable for the projector.

According to the invention, the transparent substrate having the monocrystal semiconductor layer is used to form integration of the projector light valve device. The peripheral circuit section for driving the pixel array section is integratedly formed on the monocrystalline semiconductor layer. It is of course possible to form also the pixel array section on the monocrystal semiconductor layer. The monocrystalline semiconductor layer has a high uniformity of crystal and is thermally stable, thus processing at a high temperature can freely be performed to produce the fine structure monocrystalline transistor element, simultaneously since it has a larger carrier mobility compared to the polycrystal semiconductor layer or amorphous semiconductor layer, the transistor element with a high speed response can be obtained. Therefore, compared to the conventional example, the projector light valve device with a compact size, high performance, high density, and high accuracy is produced. The video signal processing circuit and the like in addition to the driving circuit can be added to the peripheral circuit section according to the circumstances.

In addition to the foregoing basic operation, various devices are intended. For example, the light reflection shielding film is formed on the transparent substrate for shielding the individual switching elements from th incident light. The light r fl ction shi lding film not only prevents light l akage of switching el ments but also suppr ss s temp ratur ris of th light valve devic b caus of refl cting th incid nt light. Th solar c ll is int grally form d on th monocrystallin s miconductor lay r to enabl a s lf-sufficient power supply voltage and to intend effective energy utilisation for the peripheral circuit section. The light valve device contains the micro-lens array, and only the pixel electrode portion is selectively lighted to improve a utilisation efficiency of the light from the light source. The light valve device includes the cooling means to effectively suppress temperature rise.

Embodiments of the present invention will now be described with reference to the accompanying drawings, of which:

Figure 1 is a perspective view showing one embodiment of the present invention;

Figure 2 is a circuit diagram showing a further embodiment of the present invention;

Figure 3 is a circuit diagram showing an embodiment of a light source element driving circuit;

Figure 4 is a block diagram showing a television camera view finder assembled using a monocrystalline semiconductor type image display device according to the present invention;

Figure 5 is a block diagram showing a concrete structural example of a display data generating circuit and a control circuit as shown in figure 4;

Figure 6 is a block diagram showing an example of a first X driving circuit in figure 4;

Figure 7 is a circuit diagram showing one embodiment of the present invention;

Figure 8 shows a transmission circuit and a receiving circuit;

Figures 9(A) to 9(H) illustrate the process of producing the monocrystalline semiconductor type image display device according to the present invention;

Figure 10 is a schematic sectional view showing a modification example of the monocrystalline semiconductor type image display device according to the present invention;

Figure 11 is a sectional view showing an example of a light valve cell;

Figures 12(A) to 12(E) illustrate the process of producing the light valve cell;

Figure 13 is a schematic sectional view of a monocrystalline semiconductor type light valve device;

Figures 14(A) to 14(E) illustrate the process of producing the monocrystalline semiconductor type light valve device;

Figure 15 is a schematic sectional view of the monocrystalline semiconductor type light valve device incorporated unitary with a solar cell;

Figure 16 is an equivalent circuit diagram of the light valve device in figur 5;

Figure 17 is a p rspective view showing a solar cell incorporated into the light valv d vic in fig-

ur 5;
Figure 18 is a simplified view showing monocrystallin semiconductor type light valve d vic attached with a micro-lens array;
Figure 19 is a sectional view showing a monocrystalline semiconductor type light valve device attached with a micro-lens array as in figure 18;
Figure 20 is a sectional view showing an embodiment of a compact-size image display device of the present invention;
Figure 21 is a sectional view showing another embodiment of a compact-size image display device of the present invention;
Figure 22 is a sectional view showing a stereoscopic image display device of the invention;
Figures 23(A) to 23(C) are schematic diagrams showing a basic construction of an IC package type monocrystalline semiconductor light valve device according to the present invention;
Figure 24 is a sectional view showing a first embodiment of an IC package type monocrystalline semiconductor light valve device;
Figure 25 is a sectional view showing a second embodiment similarly;
Figure 26 is a sectional view showing a third embodiment similarly;
Figure 27 is a sectional view showing a fourth embodiment similarly;
Figure 28 is a sectional view showing a fifth embodiment similarly;
Figure 29 is a sectional view showing a sixth embodiment similarly;
Figure 30 is a sectional view showing a seventh embodiment similarly;
Figures 31(A) and 31(B) are sectional views showing an eight embodiment similarly;
Figure 32 is a perspective view showing a ninth embodiment similarly;
Figure 33 is a schematic sectional view showing an optically addressed type light valve cell;
Figure 34 is a sectional view showing a particular embodiment of an IC package type monocrystalline semiconductor light valve device of the present invention, where an optically addressed type light valve cell is incorporated together with a monocrystalline semiconductor light valve cell in figure 33;
Figure 35 is a sectional view showing a projector monocrystalline semiconductor type light valve device including a cooling means;
Figure 36 is similarly a schematic view showing a projector monocrystalline semiconductor type light valve device including a cooling means;
Figure 37 is similarly a schematic view showing a projector monocrystalline semiconductor type light valv d vice including a cooling m ans;
Figure 38 is similarly a schematic vi w showing a projector monocrystallin semiconductor typ light valve device including a cooling means;
Figure 39 is a schematic view showing a basical structur of a projector which us s a monocrystalline semiconductor type light valve device according to the present invention; and
Figure 40 is an entire view showing one example of the conventional active matrix type liquid crystal display device.

Figure 1 is a perspective view of a compact type image display device for illustrating an embodiment according to the present invention.

In figure 1, a monocrystalline silicon thin film 2 is adhered on a quartz glass substrate 1. An X driving circuit 6 and a Y driving circuit 8 are formed on the thin film 2 into an integrated circuit by VLSI processing. Each driving electrode 5 is formed in a matrix shape for introducing output signals of the X driving circuit 6 and Y driving circuit 8. Transistors 9 and display image electrodes 10 are arranged at intersecting points of the driving electrodes 5 in matrix shape. A control circuit 4 is provided for supplying timing signals to the X driving circuit 6 and Y driving circuit 8. A display data generating circuit 3 for generating display data for image displaying is also provided. In addition, a light source element driving circuit 19 for driving light source elements is also provided. The configuration further comprises a first transparent substrate in which a polariser 11 is adhered on the backside of the quartz glass substrate 1, and a second transparent substrate in which a polariser 13 is adhered on the backside of a glass substrate 12 provided with common electrodes 14. A liquid crystal layer 16, which is provided between the first substrate and the second substrate, is sealed by a seal agent 15. The Y driving circuit 8 is disposed on the left-side to a pixel array section 17, the control circuit 4 and the display data generating circuit 3 are disposed on the right-side. Such respective arrangements are not, however, to be taken limitatively.

In figure 1, the display data generating circuit 3 with an incorporated A/D conversion circuit inputs imaging signals of a CCD image pick-up device and the like for picking up an image of the object, and outputs display data for image displaying to the X driving circuit 6. The control circuit 4 inputs horizontal synchronisation signals and vertical synchronisation signals separated from composite signals from the CCD image pick-up device.

The control circuit 4 receives horizontal synchronisation signals and vertical synchronisation signals to output timing signals necessary for display to the X driving circuit 6 and the Y driving circuit 8. The X driving circuit 6, incorporates 4 bit display data composed of A/D converted video signal from the display data generating circuit 3, which are sequentially shifted to an incorporat d 4 bit parallel shift regist r circuit in synchronisation with the timing signals of th control circuit 4 (shift clock signals of display data).

When the display data, corresponding to the amount of one line is taken in, data corresponding to the amount of one line are latched by an incorporated latch circuit using the timing signals (data latch signals). The display data thus latched are converted into analogue signals by an incorporated D/A conversion circuit to be output to the source terminals of each transistor in the pixel array section 17. Simultaneously, to select one scanning line, the Y driving circuit 8 outputs selected voltages to one driving electrode, to turn ON each gate of the transistors and to supply an output voltage of the X driving circuit 6 to the display pixel electrode.

The liquid crystal layer 16 provides a pixel display with a variable density depending on the amplitude of the voltage applied to the common electrode 14 and the display pixel electrode 10. Thus, the Y driving circuit 8 and the X driving circuit 6 display the image signals picked-up onto the image array section 17 by linearly sequentially driving. It is understood that electro-optic materials are not limited to liquid crystal, the foregoing and other fluid materials or solid materials can suitably be used therein. In this example, a pair of substrates 1 and 12 are used so as to constitute a flat panel construction and are formed of glass material and so is of a light transmission type. However, the present invention is not limited to the above example notwithstanding, since at least one-side thereof may preferably be transparent.

The liquid crystal layer 16 is sealed in a gap between the first transparent substrate and the second transparent substrate by the seal agent 15. The seal agent 15 is made, for example, from bonding a resin of the ultraviolet hardening type, and is applied along a predetermined seal region 18 as shown by dotted lines. The seal region 18 is defined so as to overlap the peripheral circuit section embracing the pixel array section 17 positioned at the centre so as to enable a compact mounting on the flat panel. It is unnecessary to provide any particular zone between the pixel array section and the peripheral circuit section as in the conventional example. Accordingly the surface area is reduced, and the pixel array section 17, which is positioned substantially at the centre of the quartz glass substrate 1, can advantageously be assembled into the casing or housing.

Figure 1 shows one example of the monocrystalline semiconductor type light valve cell, however, the present invention is not limited to such examples. Generally, the monocrystalline semiconductor type light valve cell is a light valve device of a compact type with high accuracy wherein the driving circuit, the other peripheral circuit section and the pixel array having the monocrystalline semiconductor layer as an active region are formed on one chip. The pixel array is of an active or simple matrix type. Switching elements of the active matrix type may use amorphous silicon transistors, polysilicon transistors, diodes and the like in addition to monocrystalline silicon transistors, which are provided corresponding to the pixel electrodes respectively. In the simple matrix type, the pixel array is formed of only the pixel electrodes arranged in an intersecting manner vertically and horizontally and without switching elements. In either of these cases, the monocrystalline semiconductor type light valve elements feature formation of the peripheral circuit section into the monocrystalline semiconductor layer.

Figure 2 shows one embodiment where a compact type image display device according to the present invention is applied to a view finder of an 8mm video camera. Figure 2 shows a configuration of a CCD image pickup device 27 as an element for picking up the object image. Image pickup signals of the CCD image pickup device 27 and a composite signal of video signals and the synchronisation signals. These signals are input into the synchronous separation circuit 26 of the data signal generating circuit. The configuration comprises an A/D conversion circuit 25 for A/D conversion the video signals of the synchronous separation circuit 26, the control circuit 4 for generating the timing signals for display, the X driving circuit 6, the Y driving circuit 8, the light source element driving circuit 19 for driving the pixel array section 17 and a light source element 30.

An operation of the device of figure 2 is now described. Composite signals CD from the CCD image pickup device are input into the synchronous separation circuit 26 of the data signal generating circuit. The synchronous separation circuit 26 outputs video signals DT to the A/D conversion circuit 25. The synchronous separation unit 26 outputs horizontal synchronisation signals HSYC, vertical synchronisation signals VSYC, and clock signals CK to the control circuit 4.

The clock signals CK are a reference clock signal generated when a PLL circuit (not shown) is inputted with the horizontal synchronisation signals.

The A/D converter circuit 25 converts the video signal DT into the 4 bit digital signals to be outputted to the X driving circuit 6. The control circuit 4 generates the timing signals (data shift clock signals CL2, data latch signals CL1, frame signals FRM, and alternating-current-forming control signals M and like signals) required for operating the X driving circuit 6 and the Y driving circuit 8. The X driving circuit 6 and the Y driving circuit 8 are operated by the timing signals of the control circuit 4 to display images on the pixel array section 17. An optical element 30, such as electroluminescence EL, is disposed on the back of the transparent pixel array section, and driven by the driving circuit 19 for driving the light source element 30.

Figure 3 shows one embodiment of the light source element driving circuit 19. In figure 3, the light source element driving circuit 19 connects a transformer 31 and an electrolytic capacitor 37 to the light

source element driving circuit 19. The EL light source element 30 is connected between terminals T1 and T2 to produce oscillation by inductance L of the transformer 31 and capacitance C of the EL light source element 30. The current variation arisen therefrom induces reverse phase voltage in a secondary coil. The induced voltage is fed back to base of a transistor 32. Thus, the induced voltage is amplified and by the transistor 32 and its phase is inverted to operate for driving a load due to inductance L of the transformer and capacitance C of the EL light source element. Hence, an output voltage with a driving waveform of 400 Hz at about 100 V is output across terminals T1 and T2, and lights the EL light source element 30.

Figure 4 is a block diagram showing an example wherein the monocrystalline semiconductor type image display device according to the present invention is applied to view finders of the 8 mm video cameras. The monocrystalline semiconductor type image display device is externally connected with a CCD element 1021 and a recording/reproducing circuit 1022. The CCD element 1021 picks up the object image and outputs image signals D1. The recording/reproducing circuit 1022 is provided for recording and reproducing the image pickup signals D1.

The monocrystalline semiconductor type image display device comprises a display data generating circuit 1003, a control circuit 1004, a pair of X driving circuits 1006 and 1007, a Y driving circuit 1008, and a pixel array section 1017. The display generating circuit 1003 generates display data required for displaying pickup image information supplied from the CCD element 1021. The control circuit 1004 generates various timing signals in accordance with a synchronisation signal obtained from the display data generating circuit 1003. The X driving circuits 1006, 1007 and the Y driving circuit 1008 feed a predetermined driving voltage to a matrix driving electrode group of the pixel array section 1017 depending on the timing signals.

Colour filters of red (R), blue (B), green (G) are formed as a film on the common electrode of the pixel array section 1017, for example, by electrode position or the like in order to match individual pixel electrodes and so as to achieve a colour display. The display data generating circuit 1003, the control circuit 1004, a pair of the X driving circuits 1006 and 1007, and the Y driving circuit 1008, and the pixel array section 1017 are formed unitary on the same substrate to produce a circuit.

The display data generating circuit 1003 comprises a sample hold circuit 1031, a low-pass filter 1032, a video signal processing circuit 1033, a timing pulse generating circuit 1034, a synchronisation signal generating circuit 1035, a RGB converter circuit 1038, a data separation circuit 1039, a synchronisation separation circuit 1301, and a PLL circuit 1302.

An operation of a view finder is now described referring to figure 4. A timing pulse TP produced by the timing pulse generating circuit 1034 is input into the CCD element 1021 to cause the CCD element 1021 to output the pickup signals D1 as serial analogue data.. The sample-and-hold circuit 1031 is positioned at an input stage of the display data generating circuit 1003, and samples and holds the pickup signals D1 depending on the sample-and-hold signals SP fed from the timing pulse generating circuit 1034. The sample-and-hold circuit 1031 takes out only a video signal D2 from waveforms of the pickup signals D1, to input it into the low-pass filter 1032 of the next stage. The low-pass filter 1032 eliminates clock noise due to the sample-and-hold signals SP, to input the video signals into the video signal processing circuit 1033 of the next stage. The video signal processing circuit 1033 processes the video signals D3 in various ways. The processes include, for example, clamping, T correction, white clipping, blanking mix, pedestal, and sink mix and the like. The synchronisation signal generating circuit 1035 divides the frequency of the clock signal CLK fed from the timing pulse generating circuit 1034 to produce synchronisation signals SYC, which are input to the video signal processing circuit 1033. The video signal processing circuit 1033 combines the synchronisation signal SYC with the processed video signals D3 to produce a desired composite video signal CBD.

To record or display the object image picked up by the CCD element 1021, a switch SW is turned ON. The composite video signals CDB are transferred to the recording/reproducing circuit 1022 and recorded on a magnetic tape or the like. To display the object image on the view finder, the composite video signals CBD are input into the RGB converter circuit 1036 to be separated into a brightness signal and a colour signal. Thereafter, the signals are converted into RGB display signals and fed to the clamping circuit 1037 of the next stage. The clamping circuit 1037 is provided for clamping a direct current level of the composite video signals CBD. RGB display signals D4 thus clamped, are converted into corresponding digital display data D5 by the A/D converter circuit 1038. The digital display data D5 is split into two by the data split circuit 1039. The respective display data D6, D7 are transferred to the first and second X driving circuits 1006, 1007.

The composite video signals CBD are also input to the synchronisation separation circuit 1301, which separates the horizontal synchronisation signals HSC and the vertical synchronisation VSC from the composite video signals CBD. The horizontal synchronisation signals HSC thus separated are input to the PLL circuit 1302, which outputs the reference clock signal CK. The reference clock signal CK, the horizontal synchronisation signals HSC, and the vertical synchronisation signals VSC are input to the control circuit 1004. In accordance with the synchron-

isation signals, the control circuit 1004 generat s various timing signals required for op rating th X driving circuits 1006, 1007 and th Y driving circuit 1008. These timing signals include data shift clock signals CL2, data latch signals CL1, frame signals FRM, and alternating-current forming signals M and the like.

The pair of driving circuits 1006, 1007 and the Y driving circuit 1008 are operated in accordance with these timing signals to reproduce and display colour images on the pixel array section 1017. A pair of the X driving circuits 1006 and 1007, which are split and arranged over and under the pixel array section 1017, synchronously take two series of the display data D6 and D7 separated by the data split circuit 1039. A matrix driving electrode group is formed by the connection of the pair of the upper and lower X driving circuit 1006 and 1007 and the Y driving circuit 1008, by signal lines which intersect orthogonally with gate lines. Among a plurality of the signal lines, odd-numbered lines are connected to the first X driving circuit 1006, and even-numbered lines are connected to the second X driving circuit 1007. The switching elements positioned at each intersecting point in the matrix are electrically conducted. Thus, the desired signal voltage is applied to the corresponding pixel electrodes to active the liquid crystal for an electro-optic effect and to display the image. To reproduce once recorded image data on the view finder, the switch SW is turned OFF, then the composite video signals CBD are supplied to the RGB converter circuit 1036 from the recording/reproducing circuit 1022. Therefore, a colour image can be reproduced and displayed on the pixel array section 1017 by the same operation as that in recording.

Figure 5 is a block diagram showing a configuration of the A/D converter circuit 1038 and data split circuit 1039 from the display data generating circuit 1003 and control circuit 1004 all shown in figure 4. In figure 5 the A/D converter circuit 1038 is composed of three A/D converters 1381, 1382, 1383 corresponding to RGB, the three primary colours, respectively. Each respective colour components of the analogue display signals D4 is converted into digital parallel display data of 4 bits each. Symbols R, G, B are hereinafter used for discriminating the display data using a colour basis. The data split circuit 1039 includes shift register circuits 1391, 1392, 1393 for shifting 4 bit parallel data R, G, B, a latch circuit 1394 for temporarily latching output of the shift register circuit, switch circuits 1395, 1396, 1397 for sequentially switching output of the latch circuit 1394, and a ring counter circuit 1401 for generating timing signals SP1, SP2, SP3 in order to sequentially turn on these switch circuits. The control circuit 1004 includes a horizontal data period detecting circuit 1405 for detecting an eff ctiv data period corresponding to one line, a v rtical data period d tecting circuit 1406 for det cting an effective data period detecting circuit 1406 for det cting an effectiv data period of one frame, AND circuits 1407 and 1408, wav form shaping circuits 1402 and 1403, and a 1/2 fr quency dividing circuit 1404.

An operation of these circuits is now explained with reference to figure 5. Depending on the horizontal synchronisation signals HSC and the reference clock signal CK, the horizontal data period detecting circuit 1405 outputs a control signal which is low during a horizontal blanking period and high during a display data output period. The vertical data period detecting circuit 1406, which is input with the horizontal synchronisation signals HSC, and the vertical synchronisation signals VSC, outputs a control signal which is low during a vertical blanking period and high during a valid display data output period of one frame. The control signals obtained from the horizontal data period detecting circuit 1405 and the vertical data period detecting circuit 1406 are input to the AND circuit 1407. The output of AND circuit 1407 and the reference clock signal CK are input to the A/D circuit 1408 of the next stage. The output signal CPI of the AND circuits 1408, determines whether the RGB components of display signals D4, which are input to the A/D conversion circuits 1381, 1382, 1383, are converted into 4 bit digital data respectively. If the digital data is converted, then they are output to shifted by shift register circuits 1391, 1392, 1393 respectively. The output data of these shift register circuits 1391, 1392, 1393 are input to the latch circuit 1394.

The output signal CP1 of the AND circuits 1408 is 1/2 frequency-divided by a 1/2 frequency dividing circuit 1384 to provide output CP2. This frequency divided signal CP2 is input to the latch circuit 1394 as a latch signal. The output data of the latch circuit 1394 is input to the switch circuits 1395, 1396, 1397.

The latch circuit 1394 contains display data of R1, R2, G1, G2, B1, and B2 in sequence from right to left. This display data is transferred to three switch circuits 1395, 1396, 1397 to rearrange the data in a predetermined order. R1 is stored in right-hand side of the first switch 1395 and G1 is stored in left-hand side of the same. B1 is stored in right-hand side of the second switch circuit 1396 and R2 is stored in left-hand side of the same. G2 is stored in right-hand side of the third switch circuit 1397 and B2 is stored in left-hand side of the same. Suffix numbers 1 and 2 attached on the RGB data represent the order in which the date is transferred to the shift registers respectively. The switch circuits 1395, 1396, 1397 are sequentially switched ON by gate signals SP1, SP2, SP3 fed from the ring counter circuit 1401 to output display data D6 and D7 split into two.

The reference clock signal CK is frequency divided by the frequency dividing circuit 1409 to output the clock signal CP3 which is f d to the ring counter circuit 1401. Th display data D6 and D7 thus divid d is input to the first and s cond X driving circuits 1006

and 1007 to be sequentially shifted by pulses using the dividing clock signal CP3 as a shift clock signal CL2, thus the display data corresponding to one line is transferred. The split display data D6 is transferred to the first X driving circuit 1006 and includes R, B1, G2. The other split display data D7 is transferred to the second X driving circuit 1007 and includes G1, R2, B2. As is apparent from figure 5, this display data is split alternately into an upper and a lower section. The display data thus transferred is latched by latch signals CL1. The display data thus latched is converted to the analogue display signals by an incorporated D/A converter circuit to output to a matrix driving electrode group. The latch signals CL1 are produced by the waveform shaping circuit 1402 into which the horizontal synchronisation signals HSC is input. The other waveform shaping circuit 1403 with an input of the vertical synchronisation signals VSC generates frame signals FRM, which are fed to the Y driving circuit to become starting data for the scanning signals. The frame signals FRM are 1/2-frequency-divided by the 1/2 frequency dividing circuit 1404 to become alternating-current inversion signals M and to control polarity inversion of the driving voltage applied to the liquid crystal. Hence, alternating-current driving is performed.

As is apparent from the explanation above, the data of the analogue display signals D4 is transferred having been converted temporarily into digital display data by the A/D conversion circuit 1038. Accordingly, it is possible to effectively prevent attenuation of the signal components which may arise during data transfer. In addition, the display data is divided into two and fed to the pair of the X driving circuits 1006 and 1007. Thus, the frequency of the transfer clock can be reduced by half compared to the conventional example.

Figure 6 is a block diagram showing a configuration of the first X driving circuit 1006. The second X driving circuit 1007 also has a similar configuration. In figure 6, the X driving circuit 1006 comprises a 4 bit parallel shift register circuit 1061, a latch circuit 1062, and a D/A conversion circuit 1063. The 4 bit parallel data D6 thus input is sequentially shifted by the shift clock signals CL2. The frequency of the shift clock signals CL2 can be reduced by half as discussed above. Data corresponding to one line is transferred, then latched by the latch signals CL1. The data thus latched is level-converted. Thereafter, it is converted into the analogue display signals by the D/A conversion circuit 1063 to output a driving voltage. The D/A conversion circuit 1063 uses a high voltage HV and a low voltage LV as a driving voltage source, and controls the analogue driving voltage polarity so as to invert the driving voltage depending on the polarity on the polarity inversion signals M. The polarity inversion signals M, after being level-converted, are applied to the common electrode arranged on the opposite substrate to drive the liquid crystal alternatively.

As mentioned above, the digital data is converted into analogue signals at a final stage and thereafter applied to the liquid crystal layer. Thus, no attenuation arises at the signal transfer stage in the middle of the whole process.

Figure 7 is a circuit diagram of one embodiment according to the present invention. In figure 7, 2020 and 2021 represent CCD image pickup devices for photographing images for a right eye and a left eye respectively. 2022 and 2023 are VTR recording devices for recording image data of the image pickup devices. 2024 is an image generating device such as a video disk for generating image data for the right eye and the left eye. 2025 is a switch for switching data for selecting one of the devices. 2026 and 2027 are modulators for converting the image data into signals capable of being transmitted by radiowave RF or the like. 2028 and 2029 are amplifier circuits for amplifying the RF modulator signals. 2030 and 2031 are receiving circuits for receiving image signals which have been transmitted. 2032 and 2033 are display data generating circuits for converting the receiving signals to generating display data. 2034 and 2035 are driving circuits for driving pixel arrays sections 2036 and 2037.

An explanation will now be given when using the display elements 2036 and 2037 to obtain stereoscopic images from image signals picked up by the CCD pickup device. When switch 2025 is connected to terminal S1, then the image signals for the right eye and the left eye are input to the RF modulators 2026 and 2027. The image signals are mixed with a carrier wave by the RF modulators 2026 and 2027 and are amplified by the amplifier circuits 2028 and 2029 to transmit the image signals from an antenna (not shown). The image signals are received by an antenna (not shown) of the receiving circuits 2030 and 2031. The image signals thus received are divided into colour data to generate display data by the display data generating circuits 2032 and 2033. The display data generated by the display data generating circuits 2032 and 2033 are input to the driving circuits 2034 and 2035 to drive the image array sections 2036 and 2037. Thus the image photographed by the CCD image pickup devices 2020 and 2021 are displayed on a pixel array section for the right eye and on a pixel array section for the left eye respectively. As a consequence, a stereoscopic vision can be achieved.

Figures 8(a) and 8(b) are circuit diagrams showing a transmission-side and a reception-side of a display system for the right eye in the stereoscopic vision display device.

In figure 8(a), the RF modulator 2026 comprises; an amplifier circuit 2206 for amplifying image signals of the CCD image pickup device 2020, an AM modulating/mixing circuit 2207 for AM modulating the image signals and mixing it with carrier wave signals, a carrier wave oscillating circuit 2208 for generating

carrier wav signals, an audio signal amplifi r circuit 2202 for amplifying audio signals of a sound source 2201, a FM modulating circuit 2203 for FM modulating the audio signals, a FM modulating/mixing circuit 2204 for mixing FM modulating signals of the FM modulating circuit 2203 with the carrier wave signals, a band filter circuit 2205 for band passing an output of the circuit 2204, and a mixing low-pass filter circuit 2209 in which an output of the band filter circuit 2205 and an output of the AM modulating/mixing circuit 2207 are mixed with each other and filtered so that only low frequency signals are passed. The output signals of the mixing/low-pass filter circuit 2209 are converted into image signals to be amplified by the RF amplifier circuit 2028 and transmitted through an antenna 2221.

In figure 8(b), a tuning circuit 2210 of the receiving circuit 2030 receives image signals using a receiving antenna 2222. The image signals received by the tuning circuit 2210 are input into a carrier wave signal processing circuit 2211. The image signals are amplified, band-amplified, and input into a colour decoder circuit 2212, thus colour demodulation and colour matrix is performed to output colour video signals. A colour synchronisation circuit 2213 provides an oscillation frequency to the carrier wave signal processing circuit 2211 and the colour decoder circuit 2212. The colour synchronisation circuit uses an output obtained by giving phase detection to burst signals and crystal controlled oscillation signals. Colour outputs of red, blue and green from the colour decoder circuit 2212 are input into R-Y, B-Y, G-Y display data generating circuit 2214 and then the video signals are converted from analogue to digital. The output of the display data generating circuit 2214 is thus a digital value and inputted to an X driving circuit 2219 which is converted into analogue at each output stage to output a driving voltage by an analogue amount and to drive the pixel array section 2220.

A control circuit 2215 is provided for generating display timing signals, namely timing signals such as display data shift clock signals, frame signals, and data latch signals for driving a Y driving circuit 2218 and the X driving circuit 2219; and alternating-current inversion signals for supplying alternating-current driving inversion signals to the display data generating circuit. The Y driving circuit 2218 in a linear sequence scans and drives the Y axis driving electrode of the pixel array section 2220 to execute the image display. A light source element 2217 is arranged on the back of the pixel array section and is driven by a light source element driving circuit 2216. The light source may comprise a fluorescent tube.

The description will now turn to a method of producing the monocrystalline semiconductor type image display device according to the present invention with ref rence to figures 9(A) to 9(H). In figur 9(A), a quartz glass substrat 1101 and a silicon monocrystallin semiconductor substrat 1102 are prepared. As th substrate 1102 is pr ferably of monocrystallin silicon, a high quality of silicon wafer is used in the LSI production so that the crystal orientation thereof has a uniformity in a range of <100> 0.0 ± 1.0 with a crystal lattice defect density equal to or less than 500 pieces cm^2. First, a surface of the quartz glass substrate 1101 and a surface of the silicon monocrystalline semiconductor substrate 1102 are precisely smoothed. Following this, both surfaces, thus smoothed are piled and heated to be thermo-compression-bonded to each other. Both the substrates 1101 and 1102 are securely fixed to this thermo-compression-bonding process.

In figure 9(B), a surface of the silicon monocrystalline semiconductor substrate is ground to a desired thickness to form a silicon monocrystalline semiconductor layer 1103 on the surface of the quartz glass substrate 1101. A two layered structured composite substrate remains which comprises the quartz glass substrate 1101 eventually to become electrically insulating layers and the silicon monocrystalline semiconductor layer 1103. Instead of grinding, etching may be more preferable for obtaining the silicon monocrystalline layer 1103. In this manner the thin film of silicon monocrystalline semiconductor layer 1103 maintains the same quality of the silicon wafer so that the composite substrate has an extremely high grade crystal orientation uniformity and lattice defect density. This is in contrast to the prior art where monocrystalline thin film is obtained by re-crystallizing the polycrystal silicon thin film and so is not suitable for LSI manufacturing because of its increased lattice defects and non-uniformity of crystal orientation.

In figure 9(C), the silicon monocrystalline semiconductor layer 1103 is subject to thermal oxidation on its surface so as to deposit a silicon oxide film 1104 on the entire surface. On the silicon oxide film is deposited a silicon nitride film 1105 by chemical vapour phase epitaxy. Further thereon a resist 1106 is coated and patterned in a predetermined shape. The silicon nitride film 1105 and the silicon oxide film 1104 are etched through the resist 1106 to leave only an element region. In figure 9(D), after the resist 1106 is removed, the silicon monocrystalline semiconductor layer 1103 is thermally oxidized using, as a mask, the silicon oxide film 1104 and the silicon nitride film 1105 coating an element region, in order to form a field oxide film 1107. The silicon monocrystalline semiconductor layer 1103 remains in a region surrounded by the field oxide film 1107 to form the element region. The silicon oxide film 1104 and the silicon nitride film 1105 which were used as a mask are removed.

In figure 9(E), the thermal oxidation treatment is again executed to form a gate oxide film 1 108 in the surface of th silicon monocrystallin semiconductor layer 1103. In figure 9(F), a polycrystalline silicon film is d posited by chemical vapour phase epitaxy. This

polycrystallin silicon film is selectively tched through a resist 1110, patt rn d in a predetermined shap , to form a polycrystalline silicon gat el ctrode 1109 on the gate oxide film 1108.

In figure 9(G), after the resist 1110, is removed, impurity arsenic is ion injected through the gate oxide film 1108 using the polycrystalline silicon gate electrode 1109 as a mask to form a source region 1111 and a drain region 1112 on the silicon monocrystalline semiconductor layer. Consequently, on the lower gate electrode 1109 a channel region 1113 is formed where the impurity arsenic is not injected between the source region 1111 and the drain region 1112.

Finally in figure 9(H), a part of the gate oxide film 1108 positioned on the source region is removed to make a contact hole, to which a source electrode 1114 is connected. Similarly, a part of the gate oxide film 1108 on the drain region is removed to make a contact hole, which is covered by forming a pixel electrode 1115 thereon. The pixel electrode 1115 is composed of transparent conductive material made of indium tin oxide ITO for example. In addition, the field oxide film 1107 disposed under the pixel electrode 1115 is also transparent. The quartz glass substrate 1101 arranged further on under the field oxide film is also a transparent one. Thus, the three layered structure composed of the pixel electrode 1115, the field oxide film 1107, and the quartz glass substrate 1101 is optically transparent. In the following process (not shown in figure 9), the common electrode is adhered to the opposite electrode on which the colour filter is formed, a liquid crystal layer is filled and sealed in a gap between the two to complete the monocrystalline semiconductor type image display device.

In the embodiments explained, only the production of the TFT constituting the pixel switching elements has been shown and described. However, at the same time as the TFT is formed, the TFT in the peripheral circuit section composed of the driving circuit, the display data generating circuit, and the control circuit etc. is also formed. The present invention features the peripheral circuit section formed in the monocrystalline semiconductor layer. Hence, the pixel switching elements can be formed, of course, in the monocrystalline semiconductor layer, but instead thereof, it can be formed partially of the polycrystalline semiconductor thin film or the amorphous semiconductor thin film. In the embodiment described, the opposite substrate overlaps the substrate on the surface of which the pixel array section and the peripheral circuit section is formed to constitute the display device. However, it is understood that the present invention is not limited to such configurations. Notwithstanding, the opposite substrate can be adhered to the flat back surface after the pixel array section and the peripheral circuit s ction hav be n transf rred to the other substrates.

In the embodiment d scrib d abov , the peripheral circuit s ction in addition to th switching elem nts contained in the pix l array s ction has be n formed entirely of MOS transistors. However, d pending on circumstances, it is preferable that MOS transistors and bipolar transistors are formed on one substrate to form a peripheral circuit section. Such a composite structure can be achieved when the monocrystalline semiconductor layers are used.

Figure 10 is a schematic sectional view where NPN bipolar transistors and N type MOS transistors are formed on one substrate. In figure 10, the silicon monocrystalline semiconductor layer 1103 is formed on a surface of the quartz glass substrate 1101 with electric insulation to form the composite substrate described. A right half region thereof is formed on the N type MOS transistors, the left half region is formed on the NPN bipolar transistors. As is apparent from figure 10, the NPN transistors and the N type MOS transistors can simultaneously be formed.

First, on a N-type silicon monocrystalline semiconductor layer 1103 is provided a P-type base diffusion layer, in which an N+ type emitter (E) region is formed. AP+ type base (B) region formed in the P-type base diffusion layer and is diffused and formed at the same time with a P well of the N type MOS transistors in CMOS process. The N+ type emitter region can be formed at the same time as the N+ type source (S) region and the drain (D) region of the N type MOS transistors.

Figure 11 is a schematic sectional view showing a structural example of the monocrystalline semiconductor type light valve cell. In figure 11, the light valve cell has a flat panel construction where an upper-side substrate 4041 and a lower-side substrate 4042 are adhered by resin seal members 4043. Liquid crystal 4044 is filled and sealed in a gap between the substrates 4041 and 4042. The opposite electrode 4045 is formed entirely on an inner surface of the upper-side substrate 4041.

The lower-side substrate 4042 is a layered structure, where from a lower-side are laminated an electric insulation base member layer 4046, a bonding layer 4047, a protecting layer 4048, and an insulation film layer 4049. A silicon monocrystalline semiconductor layer 4050 patterned in a predetermined shape is formed on the back surface of the transparent insulation film layer 4049. This forms an active region to provide switching elements 4051 composed of the insulation gate field effect type transistors. Pixel electrodes 4052, formed of transparent conductive films, are pattern on a portion where the silicon monocrystalline semiconductor layer 4050 is removed.

In addition there are wiring patterns 4053 for electrically connecting the switching elements 4051 and the peripheral circuit (not shown) to each other. The wiring patterns xtend to a take-out el ctrod 4054 formed on the front surface of the insulation film layer 4049. On a front-surface of th insulation film

layer 4049 is formed a shielding film 4055 patterned corresponding to the switching elements 4051. As is apparent from figure 11, the present monocrystalline semiconductor type light valve cell is of a transfer type construction, where the pixel array section and the peripheral circuit section (not shown) are positioned on the back of the insulation film layer 4049. The present invention is not limited to such embodiments and it is of course apparent that the present invention can employ an ordinary construction in which the pixel array section and the like are formed on a front surface. In case of the transfer type, an exposed surface of the insulation film layer 4049 becomes flat. This is convenient not only for cell assembling but also for using the exposed surface as an electrode take-out region.

Figures 12(A) to 12(E) are diagrams showing one example of a method of producing a transfer type light valve cell as shown in figure 11. First in figure 12(A), a composite substrate 4061 is prepared. The composite substrate 4061 has a structure formed by achieving a silicon base member 4062 and a silicon monocrystalline semiconductor layer 4063 to each other with an insulation film layer 4064. The silicon monocrystalline semiconductor layer 4063 is adhered to a silicon bulk wafer generally used for LSI device manufacturing processes and thereafter ground and etched, to produce a thin film. Such a construction has the same high quality as that of the silicon bulk wafer.

Next, an IC process is performed in figure 12(B). The switching elements and the peripheral circuit section are simultaneously and unitarily integrated and formed. In figure 12(B), only the switching elements are shown. The silicon monocrystalline semiconductor layer 4063 is patterned in a predetermined shape and used as an active region to form switching elements 4065. The pixel electrodes 4066 patterned in a predetermined shape provided on an area where the silicon monocrystalline semiconductor layer 4063 is removed. For passivation, the above is coated with a protecting layer 4067 composed of silicon dioxide and the like. In figure 12(C), a glass substrate 4069 is adhered to the protecting layer through a bonding layer 4068 formed of silicon dioxide paste etc. In figure 12(D), the lower silicon base member 4062 is removed by etching and the underside of the insulation film layer 4064 is entirely exposed. In this way, the pixel array section and the peripheral circuit section are transferred to the glass substrate 4069 from the initial silicon base member 4062. Finally, in figure 12(E), a light shield film 4070 is patterned in a predetermined shape on the lower surface of the exposed insulation film layer 4064 to shield the switching elements 4063 from any external incident light. An opposite substrate 4072 is adhered to the insulation film layer through a resin seal member 4071, and a liquid crystal layer 4073 is filled and sealed in a gap between the two to complete a monocrystalline semiconductor type light valve cell.

Figure 13 is a sectional view showing a structural example of the monocrystalline semiconductor type light valve. The light valve has a flat panel construction formed by bonding one transparent substrate 5021 to the other transparent substrate 5022 with a predetermined gap between the substrates. A liquid crystal layer 5028 is filled and sealed in the gap. Such gap is sealed by a resin seal 5029. The lower transparent substrate 5022 is composed, for example, of glass plates and the like, and on the inside surface thereof is formed entirely an opposite electrode 5030. An outer surface is adhered with a polariser 5031.

The upper transparent substrate 5021 is of a layered structure. On the lowest layer thereof is positioned a transparent insulation film 5032, on which are integrally formed the pixel electrode 5022, switching elements 5023 and peripheral circuits (not shown) such as an X driver and Y driver and the like. Different from the ordinary construction, the present light valve is of a transfer type: a method of producing it will be described in detail later.

The present invention is not limited to the transfer type light valve. The invention can be an ordinary configuration where the pixel array section and the peripheral circuits are formed on the substrate surface.

The switching element 5023 is composed of an insulated gate electric field effect type transistor in which a silicon monocrystalline semiconductor layer 5033 is patterned in a predetermined shape and is used as an active region. A drain electrode thereof is connected to the corresponding pixel electrode 5022, a gate electrode 5034 is arranged on a channel forming region of the transistor through the gate insulation film. A wiring pattern 5035, composed of aluminium or the like, is formed on the transparent insulation film 5032. This wiring pattern 5035 is electrically connected to the source electrode of the switching element 5023, and it is further connected to a pad take-out section 5036. The wiring pattern 5035 is also electrically connected to the peripheral circuit section, though not shown.

On a surface of the transparent insulation film 5032 is formed a protecting film 5037. Further thereon a glass base member 5039 is bonded through a bonding agent layer 5038, thereby preventing damage due to mechanical stress. Still further adhered thereon is a polariser 5040.

A shielding film 5041 is pattern through the transparent insulation film 5032 so as to match the switching element 5023. The shielding film 5041 shields incident light, to prevent the switching element 5023 from maloperation, and simultaneously to suppress any light leakage current. The shielding film 5041 is coated not only on the switching element but also on the peripheral circuit section. The shielding film 5041 is made of, for example, aluminium or silver or the like and is reflective. Therefore, when it is incorporated in

the projector, the light from the source is reflected, and not absorbed. For this reason, heating due to light adsorption is suppressed and the temperature rise of the light valve is also suppressed effectively.

In this example, an additional light reflective shielding film 5042 is pattern in an interface between the bonding member layer 5038 and the glass base member 5039 to substantially shield the switching element 5023 completely from the light at the upper and the lower side and to further prevent any temperature rise.

As hereinbefore described, since the switching element 5023 is formed into the silicon monocrystalline semiconductor layer 5033 having an extremely high carrier mobility, this provides the light valve capable of high speed signal-response. The peripheral circuits, such as X driver and Y driver and the like, can be formed into one silicon monocrystalline semiconductor layer together with the switching elements 5023, thus a light valve with a high performance can be obtained. In this embodiment, a pair of polarisers 5031, 5040 are used. However, if an electrooptic material such as a polymer diffusion type liquid crystal in which the liquid crystal is diffused into high polymer material, is used instead of nematic liquid crystal having an ordinary twist alignment, then it is unnecessary to use the polarisers.

A method of producing the monocrystalline semiconductor type light valve according to the present invention is described in detail referring to figures 14(A) to 14(E). In figure 14(A), a composite substrate having a predetermined layered structure is prepared. This structure has a thin film silicon monocrystalline semiconductor layer 5053 adhered on a silicon substrate 5051 through a transparent insulation film 5052 made of silicon dioxide. The silicon substrate 5051 is provided in order to maintain mechanical strength when the monocrystalline semiconductor layer 5053 is ground or etched.

An IC process is performed in figure 14(B). The silicon monocrystalline semiconductor layer 5053 is patterned in a predetermined shape to provide an element region. The IC process is applied to the element region to integrate and form insulated gate field effect type transistors constituting switching elements 5054, or X driver, Y driver or the like at the periphery. As a result of selectively removing the silicon monocrystalline semiconductor layer 5053, the transparent conductive film such as ITO is patterned on an exposed surface portion of the transparent insulation film 5052 to provide a pixel electrode 5055. Finally, the entire substrate is coated with a protecting film 5056.

In figure 14(C), a glass substrate 5058 is adhered to the above through a bonding agent layer 5057 made of silicon dioxide. At this step, a light reflective shielding film 5059 is previously patterned on a bonding-side interface of the glass substrate 5058 so as to match switching element 5054. In figure 14(D), the silicon substrate 5051 is entirely removed by etching, to expose the back surface of the transparent insulation film 5052. In this manner, the pixel array section including the switching elements 5054, pixel electrodes 5055 etc and the peripheral circuit section (not shown) are transferred to the glass substrate 5058 from the silicon substrate 5051.

In figure 14(E), a liquid crystal cell is assembled. A light reflective shielding film 5060 is patterned on an exposed surface of the transparent insulation film 5052 so as to match with the switching element 5054. Next, an opposite glass substrate 5062 is adhered thereon through a resin seal member 5061. Finally, a liquid crystal layer is filled and sealed into a gap provided between the opposite glass substrate 5062 and the transparent insulation film 5052. An opposite electrode (not shown) is previously formed on the inside surface of the opposite glass substrate 5062. Colour filters are also layered depending upon circumstances. In the transfer construction described above, since the liquid crystal cell is assembled on the extremely flat exposed surface of the transparent insulation film 5052, one can obtain a liquid crystal panel having an improved uniformity of alignment and gap. The exposed flat surface is simultaneously used to easily form a circuit wiring pattern.

Figure 15 is a schematic sectional view showing a second embodiment of the monocrystalline semiconductor type light valve according to the present invention, showing the example of one incorporated with a solar cell. For easier understanding of figure 15, a liquid crystal cell and an opposite substrate are omitted from figure 15. A substrate, which is used for the present light valve has a layered structure, in which a transparent insulation film 5071, a silicon monocrystalline semiconductor layer 5072, a bonding agent layer 5073, and a glass base member 5074 are sequentially layered. The present example is also of a transfer type, where the pixel array section and the peripheral circuit section (not shown) are unitarily formed on the silicon monocrystalline semiconductor layer 5072. Furthermore, the present embodiment features solar cells 5075 which are composed of PN junction diodes and formed on the silicon monocrystalline semiconductor layer 5072 together with the above. A plurality of solar cells 5075 are prepared and respectively insulated against each other by element separating zones 5076 made of silicon dioxide etc. Thus, the solar cells 5075 can be connected in series, and it is possible to directly take out an output voltage of a required level. To connect the respective solar cells 5075 with each other, metal lines 5077 are patterned and provided on the element separating zones 5076. An incident light from the light source section (not shown) is received by the solar cells 5075 and photo-converted to produce a desired electromotive force.

Figure 16 is an equivalent circuit diagram of a

structure shown in figure 15 in which the solar cells 5075, formed of the PN junction diodes, are connected in series with each other by the predetermined number of pieces. An electromotive force of one solar cell is, for example, 0.7 V, and if 25 to 30 pieces of the cells are connected in series, one can obtain directly a power supply voltage of 15 to 20 V. A constant voltage regulator circuit 5078 is connected to both ends of the serially connected solar cells. A voltage detecting circuit 5079 is combined with a voltage regulating circuit 5080. These circuits can also be integrated into the silicon monocrystalline semiconductor layer. Furthermore, at both ends of the serially connected solar cells 5075, a protecting zener diode 5081 and a stabiliser capacitor 5082 are connected in parallel. Finally, a peripheral circuit 5083 of the monocrystalline semiconductor type light valve is connected inside to both ends of the stabiliser capacitor 5082 to receive the power supply voltage. In this embodiment, light from the light source is photoconverted, to self-supply the power supply voltage for the light valve, and improve the energy utilisation efficiency.

Figure 17 is a schematic view showing a pattern of the individual solar cells formed on the silicon monocrystalline semiconductor layer. In figure 17, a P type region and an N type region are disposed in a tooth comb shape to contact at a larger area thereof. The electrodes are provided along the tooth comb pattern. The element separation zones are provided by partial oxidation of the silicon monocrystalline semiconductor layer to completely separate the solar cells, thus enabling the series connection.

Figure 18 is a schematic sectional view showing a third embodiment of the monocrystalline semiconductor type light valve according to the present invention. A micro-lens array 5092 is loaded adjacent to a light valve 5091. For easier understanding of the light valve 5091, figure 18 schematically shows a non-pixel section 5094 shielded by a light reflective shielding film 5093 and a pixel section 5095 where pixel electrodes are positioned. Individual micro-lenses 5096 contained in a micro-lens array 5092 are provided so as to match the pixel section 5095. Light incident from a light source (not shown) on an entire surface of the micro-lens array 5092 is converged by the respective micro-lenses 5096, and selectively irradiates only the pixel section 5095. Therefore, the light from the light source becomes an effective light flux to irradiate the entire pixel section 5095, and do not irradiate the non-pixel section 5094. Thus, brightness of the projected image is remarkably improved. In such a construction, the amount of light absorbed by the light valve 5091 decreases corresponding to the increase in the amount of transmitted light. Thus, temperature rises can be prevented effectively.

Figure 19 is a schematic diagram showing a modified example of the third embodiment as shown in figure 18, where this has basically the same construction. For easier understanding, the corresponding reference numerals are given to the corresponding parts as those in figure 18. The difference in figure 19 is that a transparent bonding layer 5098 is provided between the micro-lens array 5092 and the substrate 5097 of the light valve 5091. The transparent bonding layer 5098 has a smaller refractive index than that of an optical member constituting the micro-lens array 5092. Hence, the condensing rate of light from the light source can be improved even further. The micro-lens array 5092 can be formed by injection moulding. Otherwise, a micro-lens array of refraction index distribution type can be employed.

Figure 20 is a sectional view of a compact sized image display device of the present invention. In figure 20, a driving circuit and a peripheral circuit etc. formed in the monocrystalline silicon thin film layer. Liquid crystal 460 is sealed into a gap between a first transparent substrate 420 having a pixel array section and a second transparent substrate 430 having a common electrode. A display element composed of polarisers 440, 410 is provided on and under the first and second transparent substrates 420, 430 respectively. An EL light source element 300 and a transformer 310, are provided inside a first seal substrate 480 of a tightly sealed type which is made of ceramic material and is fixed by a bonding agent. A connection lead electrode 490 is provided on the first seal substrate 480. The connection lead electrode 490 is connected, for example, to an input terminal electrode of AL provided on the first transparent substrate 410 by wire bonding a thin gold line 470. The second seal substrate 500 for covering the first seal substrate 480 is constructed such that a transparent substrate, such as plastic or glass, is held by an insulator 510 of plastic or ceramic materials. The first and second seal substrates 480, 500 tightly seal the display elements and the light source elements 300 in an nitrogen atmosphere by a seal agent 520.

Figure 21 is a sectional view when a compact sized fluorescent lamp (FL light source element) 400 is used as a light source element. The same numerals are given to the similar elements as those in figure 20, thus the same explanations are omitted. In figure 21, new features a metallic condenser plate 550, the FL light source element 400, a photoconductive plate 530, and a reflector 540. The FL light source element 400 is provided on lateral edge of the display element. Radiated light from the FL light source element 400 is converged by the metallic condenser plate 550 and introduced to the photoconductive plate 530. Light conducted by the photoconductive plate 530 is reflected by the reflector 540 to irradiate the display element.

The embodiments of the present invention as described above are not limited to the applications of view finders for 8 mm cameras, since they can equally be applied to home (or sidenc) monitors for crime

prev ntion, or various monitors us d in industries, and other lik applications.

Figure 22 is a s ctional view showing a mount structure of a stereoscopic image display device of the present invention. In figure 22, a display element comprises liquid crystal 2016 of electro-optic material sealed by a first transparent substrate 2401 and a second transparent substrate 2421. The display element is provided inside a casing 2402 formed of an insulator, such as ceramic material or plastic material, and fixed by a bonding agent 2415. The casing 2402 is provided with an electrode lead 2403 for introducing a power supply voltage or required electric signals, and connected to the driving circuit and the other peripheral circuit formed on the first transparent substrate 2401 by thin lines of Au wires. A lower portion of the fixed display element is composed of a light source element 2407, a photoconductive plate 2406 for conducting incident light, a reflector 2408 for reflecting light, a light condenser plate 2420 for converging light, and a light source element parts fixed on a holding plate 2409 for holding these described.

The display element is provided thereover with transparent cover materials 2413 made of glass or plastic material and a protecting frame 2412 formed of ceramic or plastic material holding the cover material 2413 and protecting the display device by covering thereabove. The protecting frame 2412 is adhered by a bonding agent 2414 to protect the display element placed within the casing 2402. The light source element parts constitute a unitary structured display device of the display elements and the light source elements by fixing mount holes 2410 of the holding plate 2409 and mount holes 2405 of the casing 2402 with screws 2411. The transparent cover material 2413 uses any of transparent materials, but lenses made of plastic or ceramic can be used to optically enlarge displays for better observation.

Figures 23(A) to 23(C) are schematic views showing a basic construction of an IC package type monocrystalline semiconductor light valve element according to the present invention. Figure 23(A) is a perspective view, figure 23(B) a section view and figure 23(C) a plan view. In figure 23(A), the element has an IC package construction of a light valve cell 4001, connector terminals 4002, and a package member 4003 which are unitarily formed. In the light valve cell 4001, only the pixel array section thereof can be visually observed from a window 4004, and the other portions are shielded by the package member 4003. The portions other than the pixel array section are completely moulded for shielding to prevent incident light into the peripheral circuit and to physically enhance the inside light valve cell. The package member 4003 is made, for example, of a moulded resin product which may be black. Oth rwise, a c ramic mould product may also be used, and in this cas , th inside light valve c ll 4001 is adh red into a unit shap by resin bonding. Th conn ctor t rminals 4002 are mad of a plurality of connector pins, and can easily be mount d on th circuit substrat by soldering tc. as in general IC device connector pins.

As shown in the section view of figure 23(B), the light valve cell 4001 is composed of a pair of substrates 4005, 4006 oppositely arranged to each other and at least either of which is transparent, and an electro-optic material 4007 arranged in a gap between the substrates. The electro-optic material 4007 can use, for example, liquid crystal or the like. The pixel array section and the peripheral circuit section for driving it are unitarily provided on an inside surface of the substrate 4006. The opposite electrode is provided on an inside surface of another substrate 4005. A colour filter can be formed overlapped with the opposite electrode depending on circumstances. The peripheral circuit section is integrally formed on the monocrystalline semiconductor layer provided on the electric insulation base member. The light valve cell having such a construction is hereinafter referred to as "a monocrystalline semiconductor type light valve cell". The light valve 4001 is completely enclosed by the package member 4003 to obtain a physically compact structure. The windows 4004 open on the upper and lower main surfaces of the package member 4003 and are fit unitarily with protecting glass members 4008 respectively. The connector terminals 4002 have one end electrically connected to the peripheral circuit section of the light valve cell 4001 and another end protruding from the package member 4003.

As shown in plan view in figure 23(C), only a pixel array section 4009 of the light valve cell is exposed from the main surface of the package member 4003 through the window 4004, and the peripheral circuit section is completely shielded from light. The pixel array section 4009 is covered by the protecting glass member 4008 as described to prevent the pixel array section from being damaged. The IC package type monocrystalline semiconductor light valve element, which may be integrated or solid, is thus very compact and has a high reliability. It is also easy to handle and has a simple mount structure. For example, the connector terminals 4002 are incorporated into a socket to simultaneously achieve mounting and electrical connection.

Various, modification, of the IC package type monocrystalline semiconductor light valve element according to the present invention are now described with reference to figures 24 to 34. The basic construction thereof is the same as the IC package type light valve element shown in figures 23(A) to 23(C), and for easier understanding, corresponding parts are given the same reference numerals as those in figures 23(A) to 23(C). In th construction in figure 24, th conn ctor terminal 4002 is provid d to protrude from th lateral nd surface of th packag member 4003

in parall l with the light valv cell 4001. Such a connector terminal arrangement is suitable for direct assembly of th IC package type light valv lem nt into a socket. The connector terminal 4002 includes a lead frame, one end of which is electrically connected to the peripheral circuit section of the light valve cell 4001 by wire bonding. In particular, it is wire connected to the take-out electrode (see 4054 in figures 12(A) to 12(E)) provided on an exposed surface of the substrate 4006 of the light valve cell 4001. The light valve cell 4001 and the lead frame are made into a unitary shape to be set in a metallic die. Thus, the package is completed by injection-moulding with mould resin which is preferably black.

In figure 25, the connector terminals 4002 are provided intersecting orthogonally to the light valve cell 4001 and protruding from the main surface on a lower side of the package member 4003. One end of the connector terminals 4002 is welded on the take-out electrode formed on the exposed surface of the substrate 4006 of the light valve cell 4001. This arrangement of the connector terminals is suitable, for example, for loading and soldering the package on the circuit substrate. As shown by dotted lines, the connector terminals 4002 can be provided protruding from the upper main surface of the package member 4003 and not only from the lower main surface thereof.

In figure 26, the package member 4003 has a thickness substantially equal to that of the light valve cell. The package member of this construction can thus be made even thinner compared to the construction as formerly described. However in this construction, the glass substrates 4005, 4006 of the light valve cell 4001 are exposed from the package member 4003 and the protecting glass member is removed.

In figure 27, the surface of the package member 4003 is made uneven. The surface area accordingly, increases compared to the construction example formerly described. The surface unevenness is provided for the purpose of heat radiation. This advantageously prevents deterioration of the light valve cell due to heat generated in the package. When assembling the IC package type light valve element into the image projector, the temperature rise in the package due to irradiation of an intensive light from the light source can effectively be prevented.

In figure 28, a cooling fin 4010 is provided on an outer surface of the package member 4003. The cooling fin 4010 can be provided at the same time of injection-moulding the package member 4003. An infrared radiation filter 4011 for reducing heat rays is attached on the windows of the package member 4003 instead of the protecting glass member. The temperature rise inside the package can more effectively be suppressed.

In figure 29, the infrar d radiation filters 4011 ar laminat d on polariser 4012 resp ctiv ly which ar disposed apart from th substrates 4005, 4006 of the light valve cell 4001. This pr vents conduction of absorb d h at by th infrared radiation filter 4011.

In figure 30, the construction shown in figure 29 is improved even further so as to considerably raise the cooling effect. Through holes 4013 are provided in the package member 4003 to form a path for coolant. The coolant is blasted by force with a fan 4014 or the like, and passes through the through holes 4013 to travel through a gap between the light valve cell 4001 and the polariser 4012 so as to be discharged. This enables the light valve cell 4001 to be cooled using gas.

In a coolant such as figures 31(a) and 31(B), the package member 4003 in figure 31(A) includes a recess portion 4015 releasably containing the light valve cell. In the construction example, only the connector terminals 4002 and the protecting glass member 4008 are previously unitarily moulded by resin to prepare the package member 4003. Electrode pads 4016 for being connected to the connector terminals 4002, are provided at predetermined positions of a stepwise portion in the recess portion 4015. In figure 31(B), the light valve cell 4001 is fitted in the recess portion 4015 to complete the package with extreme ease. With the light valve cell 4001 inserted, the take-out electrode provided on the substrate 4006 and the pads 4016 described above, contact each other to provide electrical connection. This construction, unlike the examples previously explained, is exchangeable like a cassette type because the package member 4003 and the light valve cell 4001 are not made into a unitary shape obtained by adhesion or moulding.

The construction in figure 32 is basically the same as that in figures. 31(A) and 31(B). In this example, the construction of the package member 4003 is more simplified. A light valve cell unit, which previously was attached with the polariser or protecting glass or the like, is inserted, as it is, into the recess portion 4015. In this example, the light valve cell or the panel can be freely exchanged. When a light cell is used by writing previously therein display data, the device can be used as in a slide projector.

Finally, an IC package construction is described, in which a monocrystalline semiconductor light valve cell of an electrically addressed type and the light valve cell of an optically addressed type are unitarily assembled. For easier understanding of this construction, an optically addressed type light valve cell 4017 is explained referring to figure 33. The optically addressed type light valve cell 4107 has a flat panel structure in which liquid crystal 4171 is sandwiched between a pair of transparent substrates 4172 and 4173. The liquid crystal 4171 can be a ferroelectric liquid crystal having a memory charact ristic. A write light is incid nt on an ut r surface of th transparent substrat 4172, and a read light is incident on out r

surface of th other transparent substrat 4173. Th inn r surface of the write-sid substrat 4172 is laminat d s quentially with a transparent substrat 4174, a photoconductive film 4175, formed of amorphous silicon and the like, a dielectric mirror film 4176, an alignment film 4177. On the inner surface of the read-side substrate 4173 is formed sequentially a transparent substrate 4178 and an alignment film 4179. The ferroelectric liquid crystal 4171 sandwiched by the alignment films 4177 and 4179 exhibits a bistable state. Such bistable state can be switched by applying a voltage.

The write light is irradiated whilst a predetermined voltage is applied to the pair of transparent electrodes 4174 and 4178. Then the resistance of the photoconductive film 4175 varies locally and an effective voltage exceeding a threshold value is applied to the ferroelectric liquid crystal 4171 to enable switching to the stable state. In this way, image information is written into the ferroelectric liquid crystal 4171. This optically addressed type light valve cell exhibits considerable high accuracy and has a resolution close to that of photography film. To read out the written image information, linearly polarised read light is irradiated. The read light passes through the ferroelectric liquid crystal 4171 to be modulated and then is reflected by the dielectric mirror film 4176. This reflection light is detected as a change in light intensity by passing through the polariser (not shown).

Figure 34 shows a package structure in which the above-mentioned optically addressed type light valve cell and the electrically addressed type monocrystalline semiconductor light valve cell are assembled adjacent to each other. The optically addressed type light valve cell 4017 is disposed substantially at a centre portion of the package member 4003. The monocrystalline semiconductor light valve cell 4001 is arranged at the read-side. One surface of the light valve cell 4001 is arranged thereon with a layer of the infrared radiation cut filter 4011 and polariser 4012, and the other surface is arranged thereon with another polariser 4012. A beam splitter 4018 is assembled on the read-side of the optically addressed type light valve cell 4017. The polarisers 4012 are attached on the read light input-side and the read light output-side of the beam splitter 4018 respectively.

The electrically addressed type light valve cell 4001 and the optically addressed type light valve cell 4017 are combined with each other to obtain various functions and advantages. For example, image information can be written into the liquid crystal light valve cell 4017 through the monocrystalline semiconductor light valve cell 4001 by electric signals. When ferroelectric liquid crystal material is used for the liquid crystal light valve cell 4017, the liquid crystal light valve cell 4017 can op rat as a memory d vice. Although the light valve cell 4017 as a singl unit provides only optical addressing, when combining it with th light valv cell-4001, th n lectrically addressing is available. In other words, control of the read light can b p rformed by lectric signals. The ferro lectric light valve cell 4017 can record image information even by a weak write light. Therefore, a monocrystalline semiconductor light valve cell 4001 arranged in front of it does not require durability for intensive light. In the construction in figure 34, when the intensity of the read light input is higher, light intensity amplification is available. Thus, it is advantageously applied to a compact type projector and the like.

The image displayed on the monocrystalline semiconductor light valve cell 4001 is collated with the image recorded in the optically addressed type light valve cell 4017 to enable optical parallel processing. This therefore processes a large amount of information over a short time. Hence, such cells can be applied to an optical computer. As hereinbefore described, the light valve cell using the ferroelectric liquid crystal has a considerable high accuracy, and to sufficiently utilise its capability, a highly precise panel as an electrically addressed type light valve cell is required. Pixel size must be equal to or less than 5 to 10 μm. In this respect, the monocrystalline semiconductor type light valve cell 1 is the only device capable of satisfying such conditions. In figure. 34, the liquid crystal light cell 4017 and the monocrystalline semiconductor light valve cell 4001 are constructed with a single body type device. However, the monocrystalline semiconductor light valve cell 4001 can be separated from the liquid crystal light valve cell 4017 by interposing a condensing lens.

A projector light valve including various cooling means is described as an example of the present invention referring to figures. 35 to 38. In figure 35, a cooling means includes an adiabatic container 5101 containing a monocrystalline semiconductor type light valve 5100. The adiabatic container 5101 includes an inlet port 5102 for introducing compressed gas and an outlet port 5103 for discharging depressured gas to effectively perform adiabatic expansion cooling. The compressed gas is supplied, for example, from a pump and the depressured gas is absorbed through a vacuum system.

In figure 36, the cooling means comprises fans 5104 for blowing the cooling gas to the monocrystalline semiconductor type light valve 5100. The fans 5104 are provided on both-sides of the light valve 5100 respectively to force the cooling gas toward the light valve 5100. Thus, blown cooling gas is introduced along guides 5105 to effectively cool both the upper and lower surfaces of the light valve 5100.

In Figure 37, the cooling means comprises a container 5106 containing the light valve 5100 and a cooling system connected to the container 5106 and supplying cooling gas. Th cooling system is compos d of a pump 5107 and piping 5018 for introducing th cooling gas. Both ends of th piping 5108 are coupl d

to the container 5016, and function as an introducing port and a discharging port. The discharging port-side of the piping 5108 is attached with a temperature sensor 5109, and temperature control of the cooling gas is automatically performed by feedback control. For this temperature sensor 5109, for example, a Peltier element can be used. An amount of gas blown by the pump 5107 is controlled depending on an output of the temperature sensor 5109.

Finally, the cooling means in figure 38, as in figure 37, is composed of a container 5110 containing the light valve 5100 and a cooling system 5111 coupled to the container 5110 and supplying the cooling gas. The difference from that in figure 37 resides in that both the introducing port and the discharging port of the cooling system 5111 are provided on one lateral surface of the container 5110. This construction means that the cooling structure of the light valve 5100 can be made compact.

Figure 39 is a schematic diagram showing a basic structure of a projector according to the present invention.

The projector is composed of a light source section 5001, a light valve 5002, and a projection optical system 5003. The light source unit 5001 includes a lamp 5004 and a reflector 5005, and lights the light valve 5002 through a condensing lens 5006. The projection optical system 5003 includes an enlargement lens or the like, which enlarges the light passed through the light valve 5002 to project it forwardly and the image is displayed on a screen 5007.

As hereinbefore fully described, the present invention enables the monocrystalline silicon semiconductor thin layer to be formed on the glass substrate, and so using fine semiconductor techniques, display elements can be constituted at a high density on the one substrate including not only the pixel electrodes, switching transistors, driving circuits, and peripheral circuits, but also the driving circuits and the bright source elements. Thus, the display elements and the light source elements are formed into one tightly sealed type unitary shape. Therefore, it is unnecessary to mount the peripheral circuits and the driving circuits of light source elements on another circuit substrate. This means that there is a reduction in the number of connections across the circuits, an improvement in reliability due to the tightly sealed construction, advantages of easier handling and the like, in addition to great improvements in cost reduction, miniaturisation and thinning.

Thus, for the peripheral circuit section, the control circuit for generating timing signals, display data generating circuit for generating display data, in addition to the driving circuit can be incorporated on one substrate. Hence, an extremely highly accurate and high-speed d active matrix type image display device can be formed.

Further according to the present invention, the peripheral circuits other than the driving circuits are arranged in a gap space between the driving electrodes from each X and Y driving circuits. Thus, enabling greater down-sizing of the first substrate, an improvement in the number of pieces obtained from one wafer, and a reduction in cost and so forth.

If the present invention is mounted in a device suitable for wearing such as a helmet or a hair band type for providing stereoscopic vision by both eyes, the stereoscopic image display device can be made wireless. The use of the present invention in this way, eliminates the problem of distance between the device and the image signal source and so provides easier handling. Moreover, the display elements and the light source elements can be unitarily formed. Hence, it is unnecessary to mount the peripheral circuits and the driving circuits for light source elements on other substrates, which brings about a reduction in the number of connections across the circuits, high reliability due to the tightly sealed construction, advantages of easier handling and the like, in addition to great improvements in costs and greater miniaturisation and thinning.

For example, the monocrystalline semiconductor type image display device according to the present invention can directly be connected to the outer CCD image pickup element, and so is suitable for the view finder of video cameras and the like. The X driving circuits are arranged separately in upper and lower portions relative to the image array section. Thus, the transfer speed of shift clock signals for transferring display data is reduced by half so as to achieve a lower power consumption. The X driving circuit converts digital display data into analogue display signals in an output stage to drive the image array section. Thereby, the image can be reproduced with a high fidelity without attenuation of any signal component. The peripheral circuits section, such as the driving circuits, control circuits, and display data generating circuits are arranged at four edges of the substrate so as to surround the image array section at a centre portion. Moreover, the seal region is regulated on the peripheral circuit portion surrounding the image array section so as to be overlapped therewith when viewed horizontally. Thus, a centre position of the image array section is substantially coincident to the centre position of the substrate to improve handling on construction and to enable miniaturisation and integration. The features that enable the device to be developed not only for view finders but also for various compact size monitors etc.

According to the present invention, the monocrystalline semiconductor type light valve cell, connector terminals, and package members are unitarily formed to produce an IC package construction. Thereby, the light valve cell can be compactly mounted and produces sufficient physical strength. Electrical connection can be simplified by incorporating th

conn ctor terminals into sock ts etc. When th light valv cell is compl tely sealed by package memb rs, th r liability is improved. Only the imag array s ction of the light valve cell is exposed and the peripheral circuit section is shielded by a package member, so that a substantially complete shield effect is obtained. A heat radiation means is provided on the packing member to produce a cooling effect.

Further, the present invention constitutes an image projector using the monocrystalline semiconductor type light valve. In the monocrystalline semiconductor type light valve, the image array section and peripheral circuit section can be arranged in a fin even more than compared with the active matrix type image display device which uses the conventional monocrystalline semiconductor thin film or amorphous semiconductor thin film. Accordingly, an extremely high accuracy of projection image can be obtained. The light reflection material is used as a shield film for coating the circuit element region of the light valve to effectively suppress temperature rise of the light valve by partially reflecting light from the light source. The solar cell is formed into a unitary shape in the monocrystalline semiconductor layer to self-supply a power supply voltage to the light valve itself by utilising energy from the light source. The microlens array matching with the pixel section, is incorporated to selectively condense the light from the light source only into the pixel section and to improve the brightness of the projection image and also to suppress a temperature rise. Furthermore, the cooling means is added to the light valve to suppress a temperature rise caused by light irradiation from the light source.

Claims

1. A light valve device comprising: a first (1) and second (12) substrate having an electrooptical material (16) therebetween; a pixel section.formed on said first substrate and which includes an X electrode group (5), a Y electrode group (5) crossing the X electrode group, and a thin film transistor (9) and a pixel electrode (10) at each cross-section of the X electrode group and the Y electrode group; and a driving circuit section which includes an X electrode driving circuit (6) for supplying display data signals to the X electrode group, and a Y electrode driving circuit (8) for supplying scanning signals to the Y electrode group, the electrooptic material forming a number of cells which are excited when the display data signals and the scanning signals selectively energises the pixel electrode through the thin film transistor, charact rised by a monocrystalline thin film (2) form d on said first substrat and in that said driving circuit s ction is formed in th semiconductor monocrystallin thin film.

2. A light valv device as claimed in Claim 1, wherein a control circuit (4) is formed on the first substrate, and timing signals are output to the driving circuit from the control circuit.

3. A light valve device as claimed in Claim 1 or 2, wherein a display data generating circuit (3) is formed on the first substrate, and the display data generating circuit inputs image signals to output display signals to the driving circuit section.

4. A light valve device as claimed in Claim 3, wherein the display data generating circuit further comprises a RGB conversion circuit, a synchronisation separation circuit (26), and the control circuit,

the RGB conversion circuit inputs the image signals to output RGB display signals to the driving circuit section, the synchronisation separation circuit outputs synchronisation signals to the control circuit, and the control circuit outputs timing signals to the driving circuit section.

5. A light valve device as claimed in Claim 3 or 4, wherein the display data generating circuit further comprises an A/D conversion circuit (25), the A/D conversion circuit converts the image signals in the form of video signals into digital video signals,

the driving circuit section includes a D/A conversion circuit (1063), the D/A conversion circuit converts digital display signals into analogue display data signals.

6. A light valve device as claimed in any one of the preceding claims, wherein the driving circuit section includes two X electrode driving circuits, the two X electrode driving circuits are disposed on either side of the pixel section respectively on the first substrate.

7. A light valve device as claimed in any one of the preceding claims, wherein the first substrate and the second substrate are adhered at a seal region which provides a gap between the two substrates with the electrooptic material sealed in the gap, and the seal region is formed so as to at least overlap the driving circuit section.

8. A light valve device as claimed in any one of the preceding claims, wherein a light source element (2217) is formed on the back of the electrooptic cell, a light source element driving circuit (2216) for driving the light sourc l ment is formed on the first substrat , and intensity of light irradiat d on th electrooptic cell is controll d by th light

source l ment driving circuit.

9. A light valv d vice as claimed in any on of the preceding claims, wherein the electrooptic cell is integrally contained in a package section (4003) having connector terminals (4002) and a window (4004) which is formed on the package section corresponding to the pixel section of the electrooptic cell, and the connector terminals and the electrooptic cell are electrically connected to each other.

10. A light valve device as claimed in claim 9, wherein the package section is formed of a non-light-penetrating material, the window section is formed of a light-penetrating material, and the driving circuit section on the first substrate is formed on a peripheral portion of the electrooptic cell and shielded by the package section.

11. A light valve device as claimed in claim 10, wherein the window section is mounted with an infrared ray filter for cutting off infrared ray.

12. A light valve device as claimed in any one of claims 9, 10 or 11, wherein the package section includes cooling means in the form of fins (4010) on its outer surface or through holes (4013) through which coolant flows in and out for cooling the electrooptic cell.

13. A light valve device as claimed in any one of the preceding claims, wherein a micro-lens array (5092) is disposed in an outer portion of the electrooptic cell.

14. A light valve device as claimed in claim 13, wherein the micro-lens array comprises a number of micro-lenses (5096) each disposed corresponding to a respective pixel electrode of the pixel section, and incident light is converged by the micro-lens to irradiate on the pixel electrode.

15. A light valve device as claimed in claim 14, wherein the micro-lens array is adhesively fixed to the electrooptic cell by a transparent bonding agent (5098), a refractive index of the transparent bonding agent is smaller than that of the micro-lens array.

16. A light valve device as claimed in any one of the preceding claims, wherein the light valve device further comprises an optically addressed type light valve cell so that light irradiated on the electrooptic cell displays an image which is projected on the optically address d typ light valv cell, and th proj cted image is stored in the optically address d typ light valv cell.

17. A light valv d vice as claimed in claim 16, wherein f rro lectric liquid crystal is sandwiched by a pair of transpar nt substrat s in the optically addressed type light valve cell; on an inner surface of at least one transparent substrate are formed a transparent electrode layer, a photoconductive film, a dielectric mirror layer, and an alignment film for aligning the ferroelectric liquid crystals sequentially from the substrate surface; and on an inner surface of the other substrate are formed, a transparent electrode layer and an alignment film sequentially from the substrate surface.

18. A binocular stereoscopic image display device, comprising a light valve device as claimed in any one of the preceding claims in which the X electrode groups are latticed so that adjacent electrodes are from different groups.

19. An image projector comprising: a light source (5004), a projection optical system (5003); and a light valve device as claimed in any one of the claims 1 to 17.

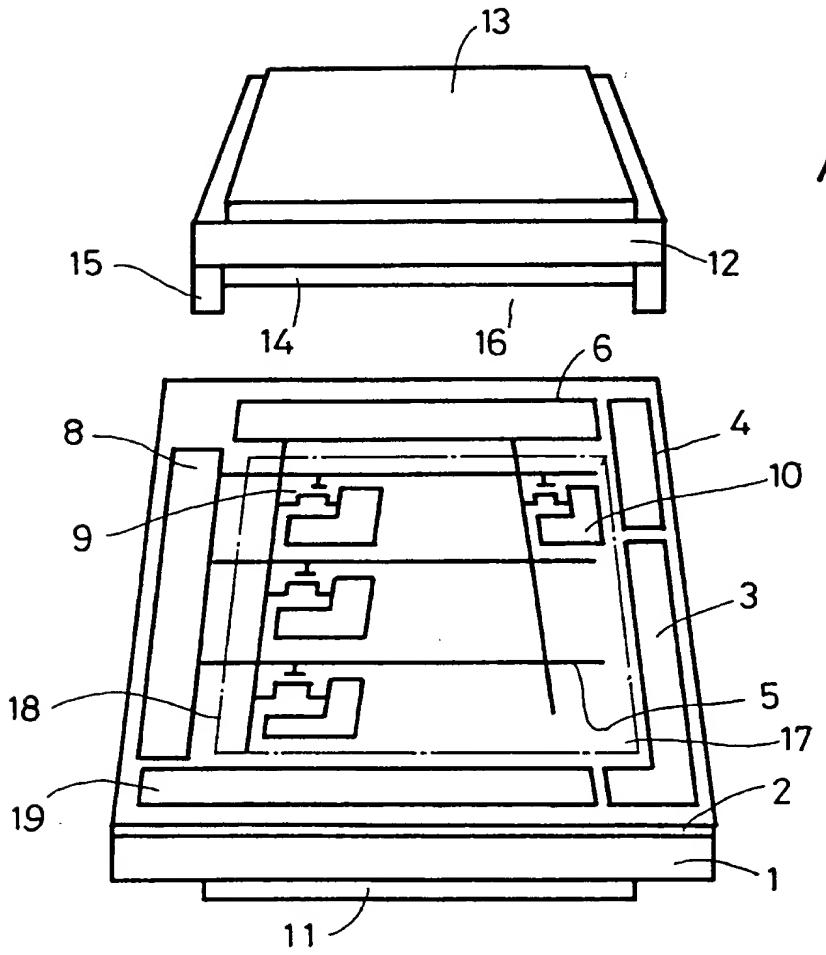


FIG. 1

FIG. 2

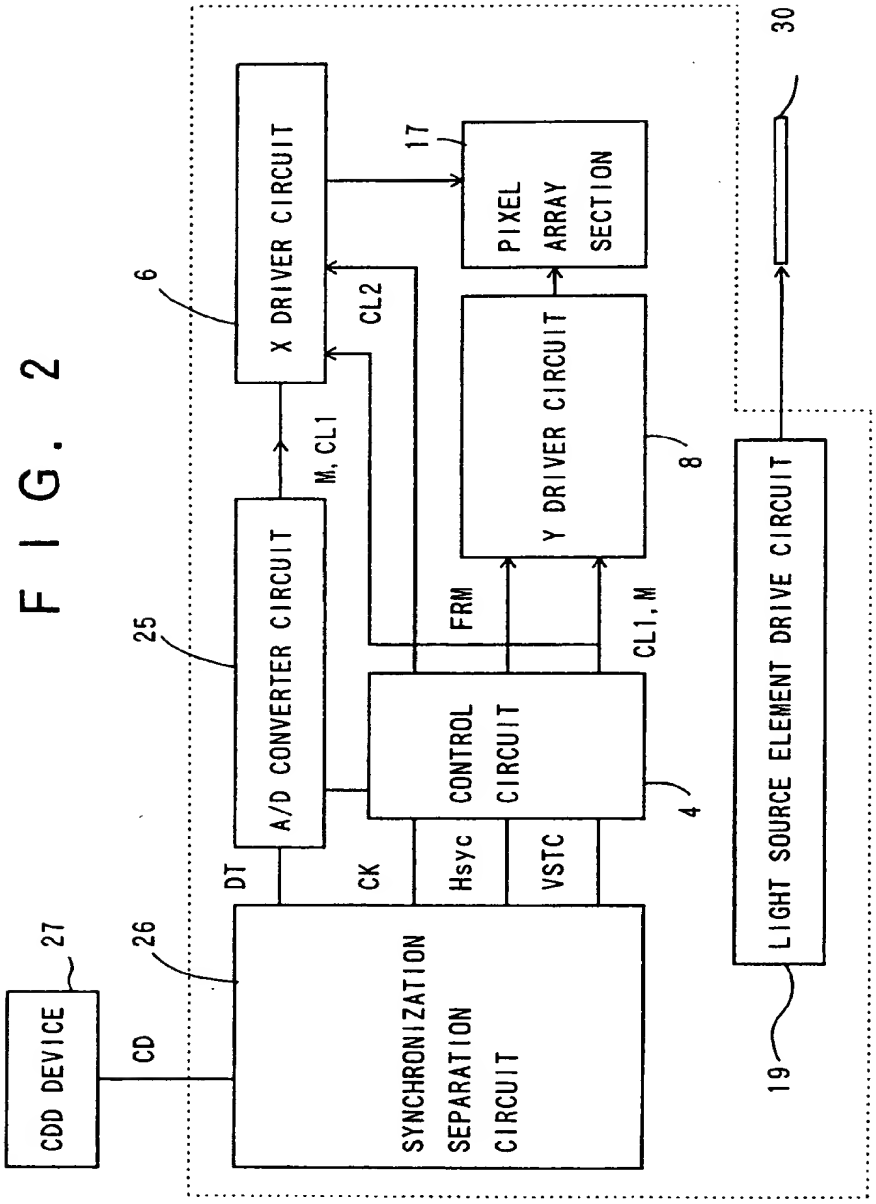

CDD DEVICE
27
CD
26
SYNCHRONIZATION SEPARATION CIRCUIT
DT
CK
Hsyc
VSTC
A/D CONVERTER CIRCUIT
25
M, CL1
X DRIVER CIRCUIT
6
CL2
17
PIXEL ARRAY SECTION
CONTROL CIRCUIT
4
FRM
CL1, M
Y DRIVER CIRCUIT
8
30
LIGHT SOURCE ELEMENT DRIVE CIRCUIT
19

FIG. 3

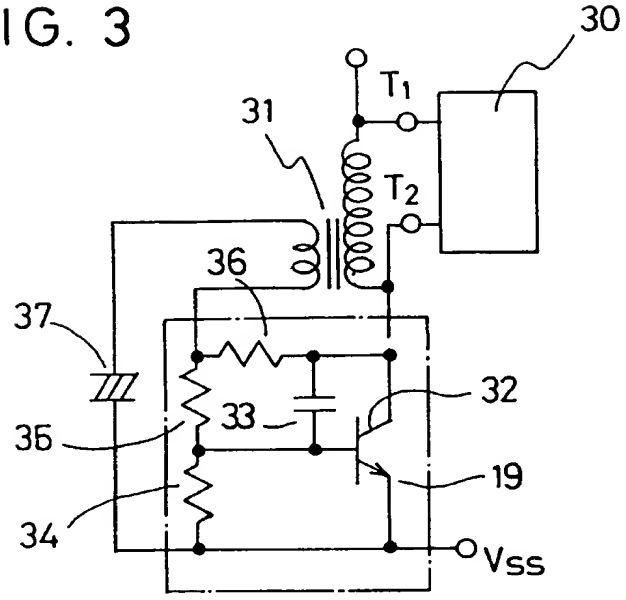


FIG. 4

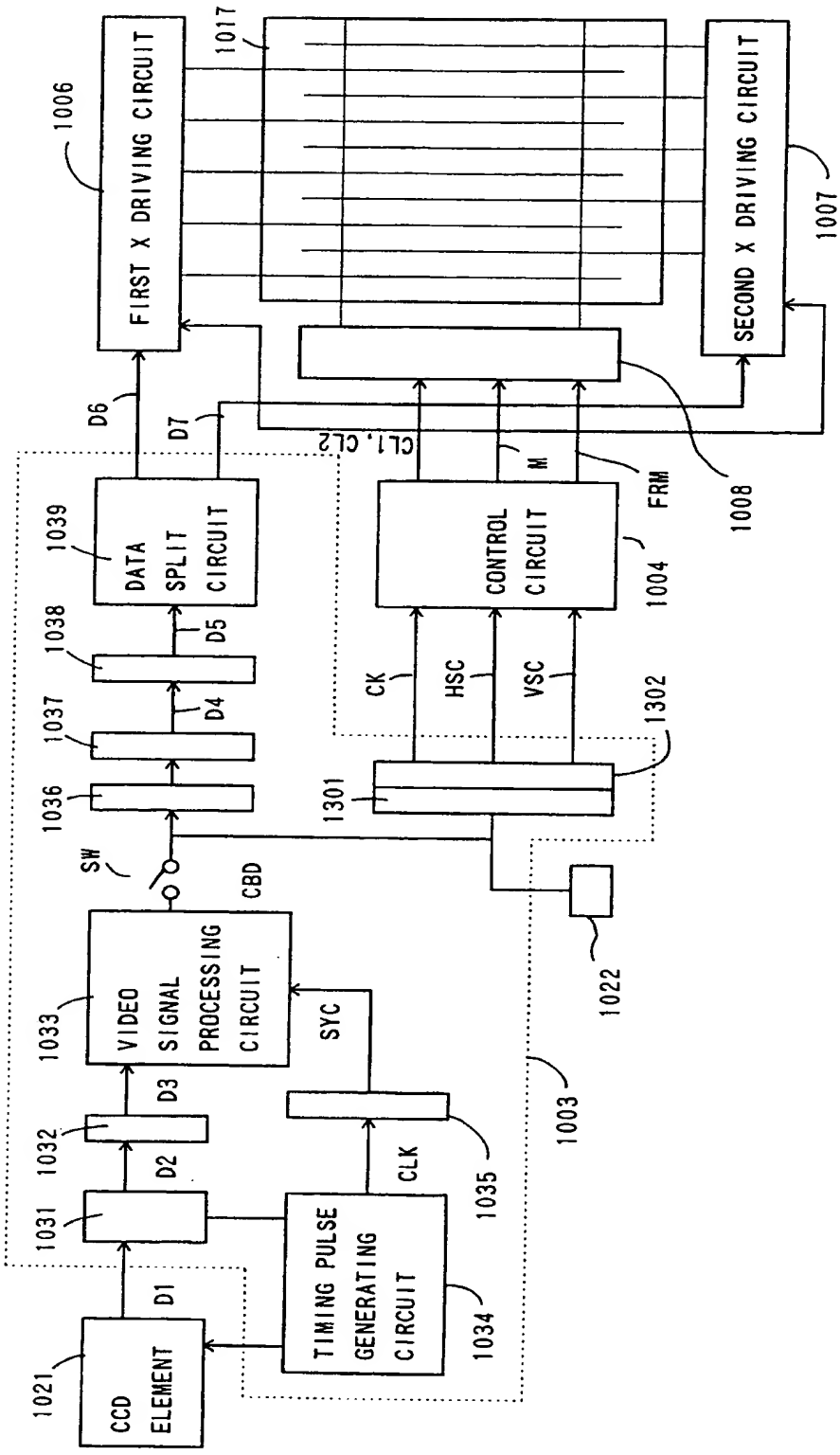
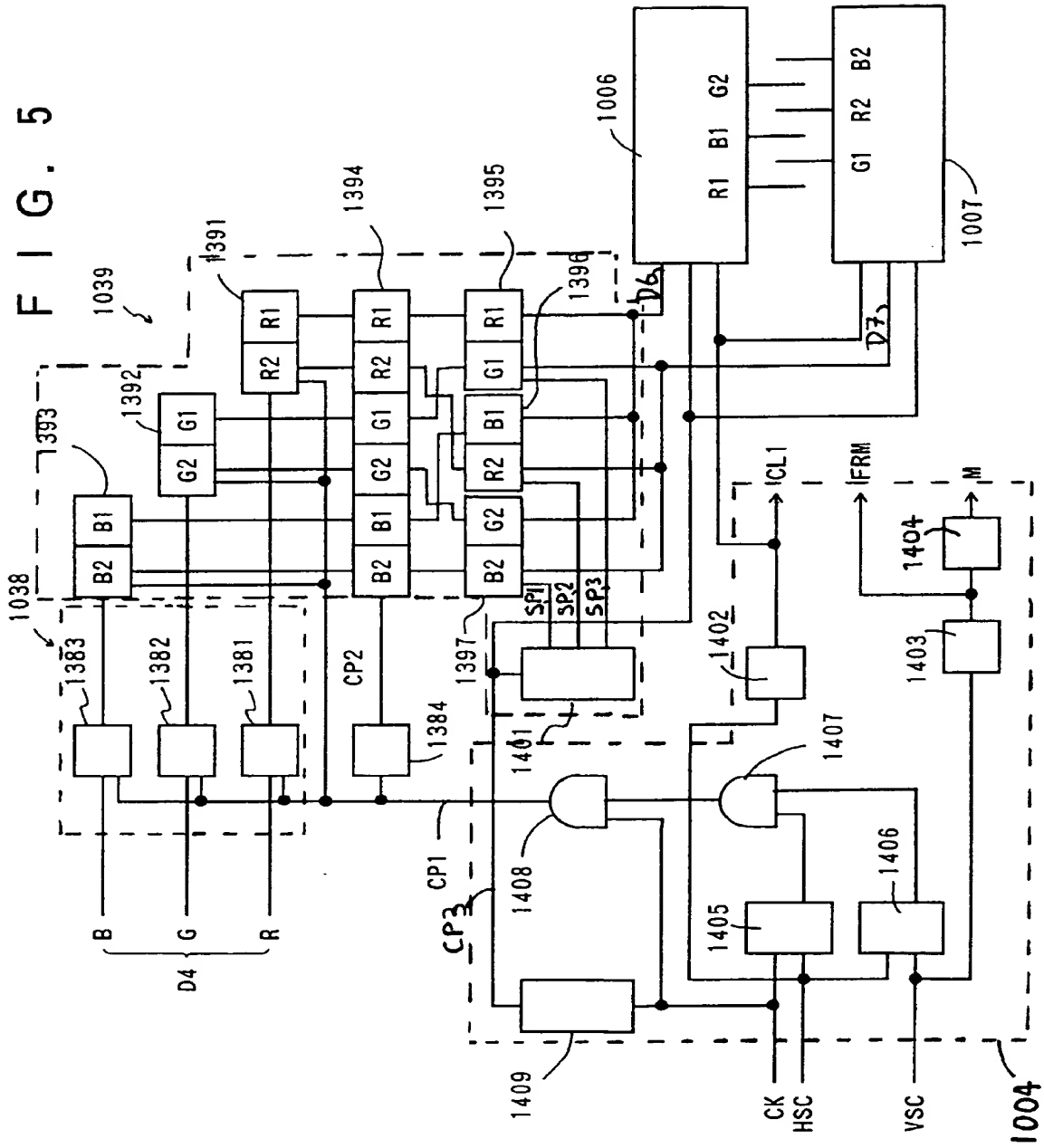

1006
FIRST X DRIVING CIRCUIT
1017
SECOND X DRIVING CIRCUIT
1007
D6
D7
CL1, CL2
M
FRM
1008
1039
DATA SPLIT CIRCUIT
CONTROL CIRCUIT
1004
1038
D5
CK
HSC
VSC
1037
D4
1302
1036
1301
SW
CBD
1033
VIDEO SIGNAL PROCESSING CIRCUIT
SYC
1022
1003
1032
D3
1031
D2
CLK
1035
D1
TIMING PULSE GENERATING CIRCUIT
1034
1021
CCD ELEMENT

FIG. 5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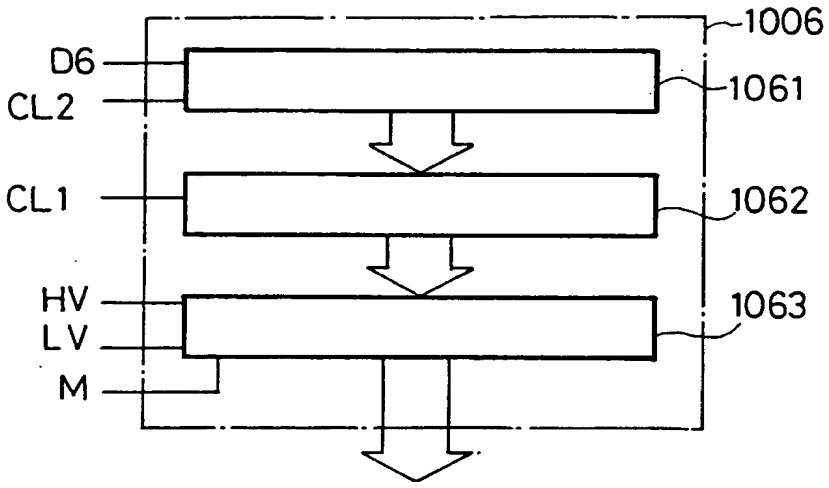
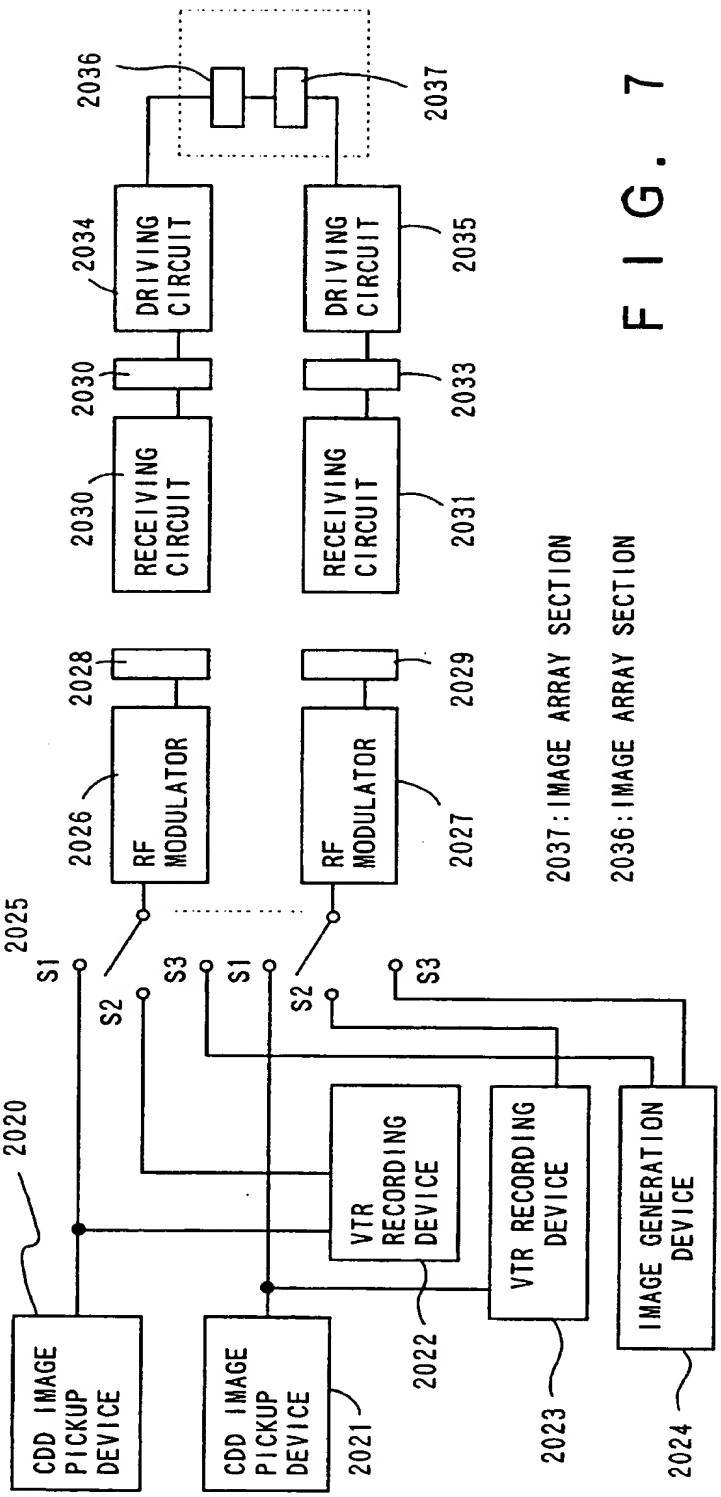
1382
1383
1384
R1
R2
G1
G2
B1
B2
CP1
CP2
CP3
SP1
SP2
SP3
D4
D6
D7
B
G
R
CK
HSC
VSC
ICL1
IFRM
M

FIG. 6




CDD IMAGE PICKUP DEVICE
CDD IMAGE PICKUP DEVICE
VTR RECORDING DEVICE
VTR RECORDING DEVICE
IMAGE GENERATION DEVICE
RF MODULATOR
RF MODULATOR
RECEIVING CIRCUIT
RECEIVING CIRCUIT
DRIVING CIRCUIT
DRIVING CIRCUIT
2020
2021
2022
2023
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2030
2031
2033
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S1
S2
S3
S1
S2
S3
2037: IMAGE ARRAY SECTION
2036: IMAGE ARRAY SECTION

FIG. 7

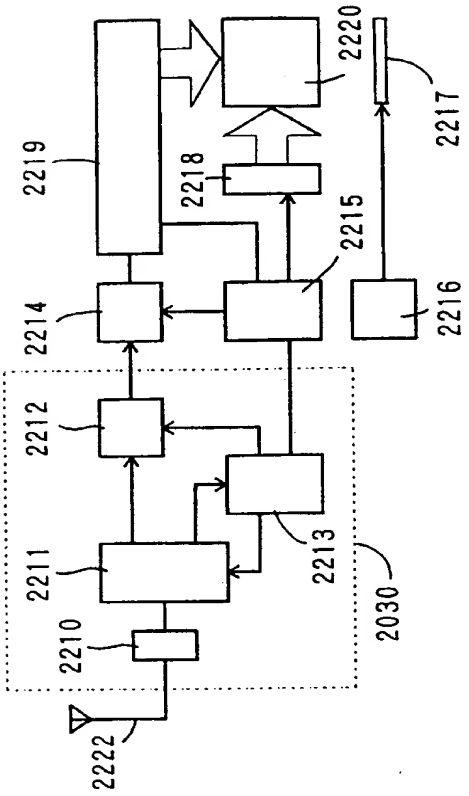
2220
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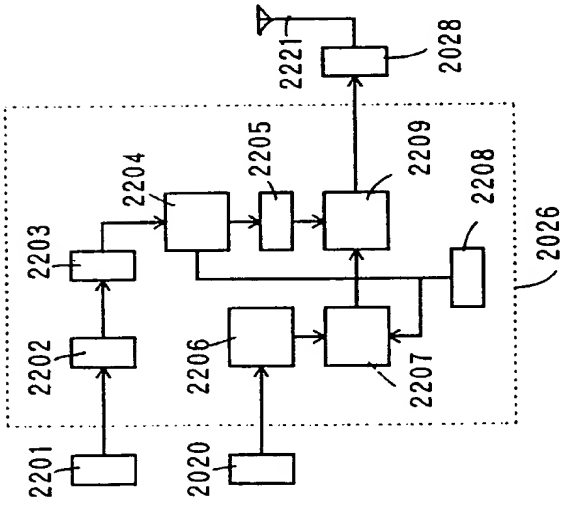
FIG. 8(b)


2221
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2207
2201
2020

FIG. 8(a)

FIG. 9(A)

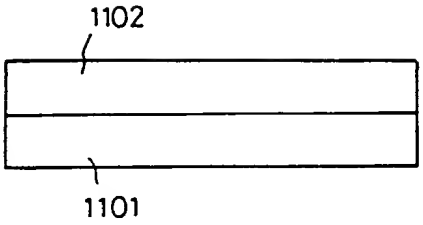


FIG. 9(B)

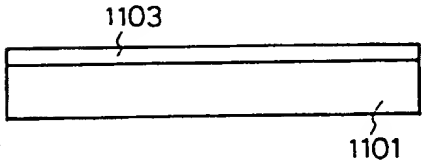


FIG. 9(C)

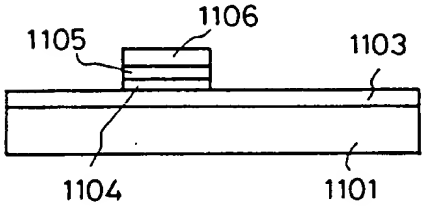


FIG. 9(D)

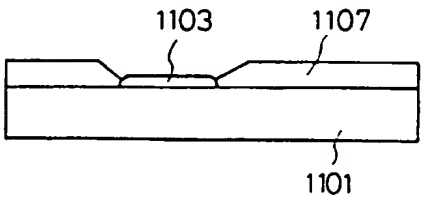


FIG. 9(E)

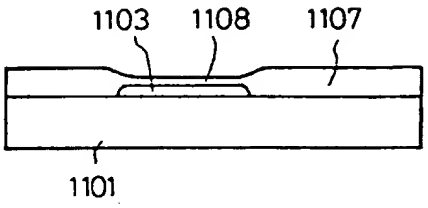


FIG. 9(F)

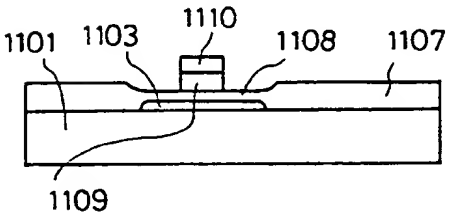


FIG. 9(G)

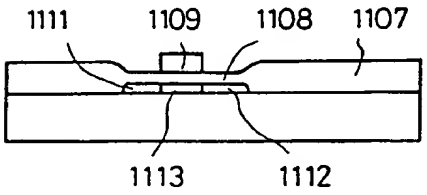
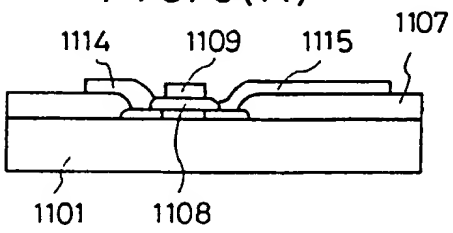


FIG. 9(H)



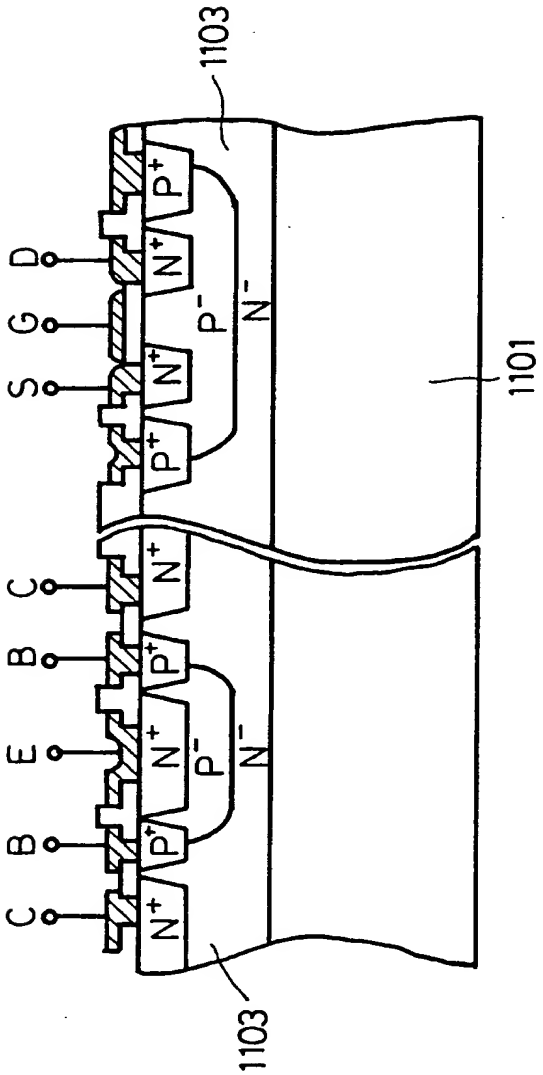


FIG. 10

FIG. 11

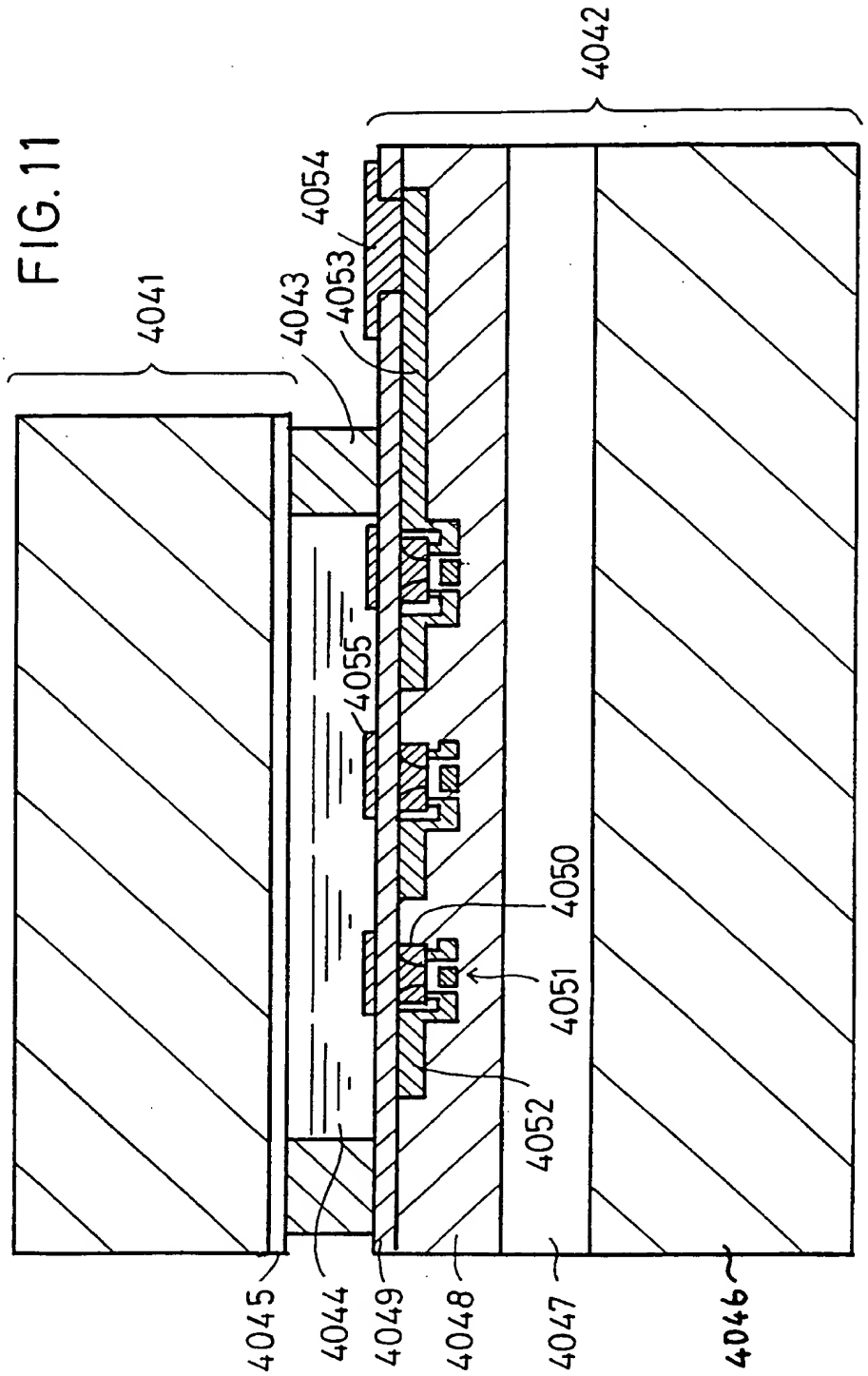

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FIG.12(A)

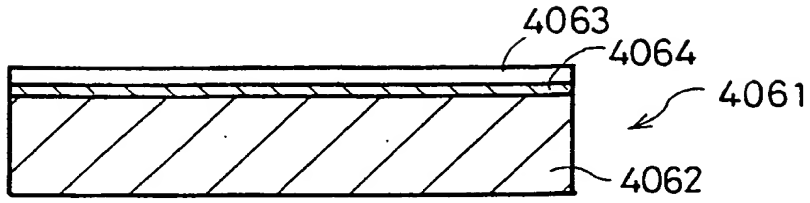


FIG.12(B)

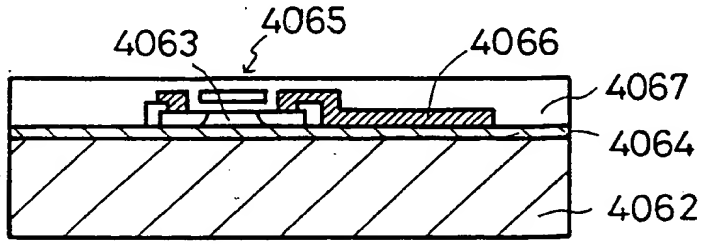


FIG.12(C)

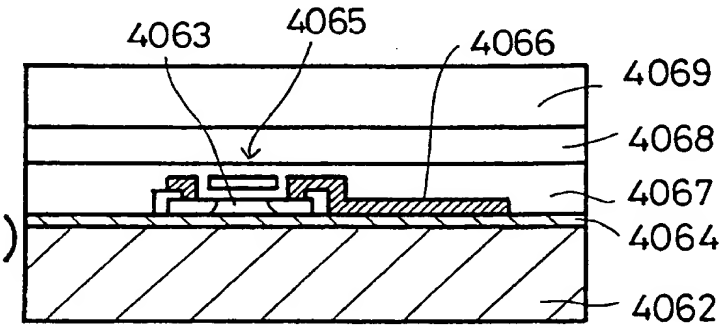


FIG.12(D)

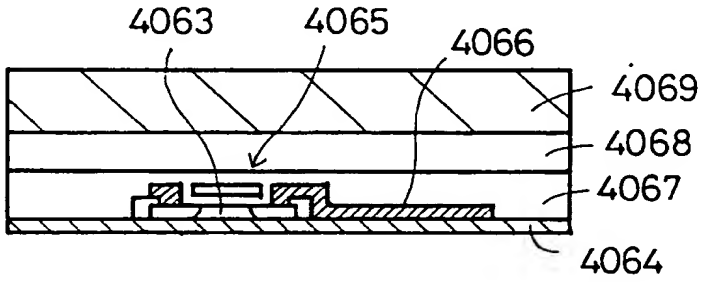
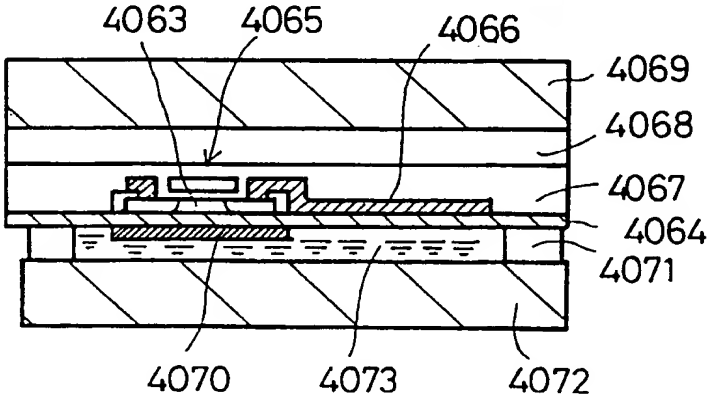


FIG.12(E)



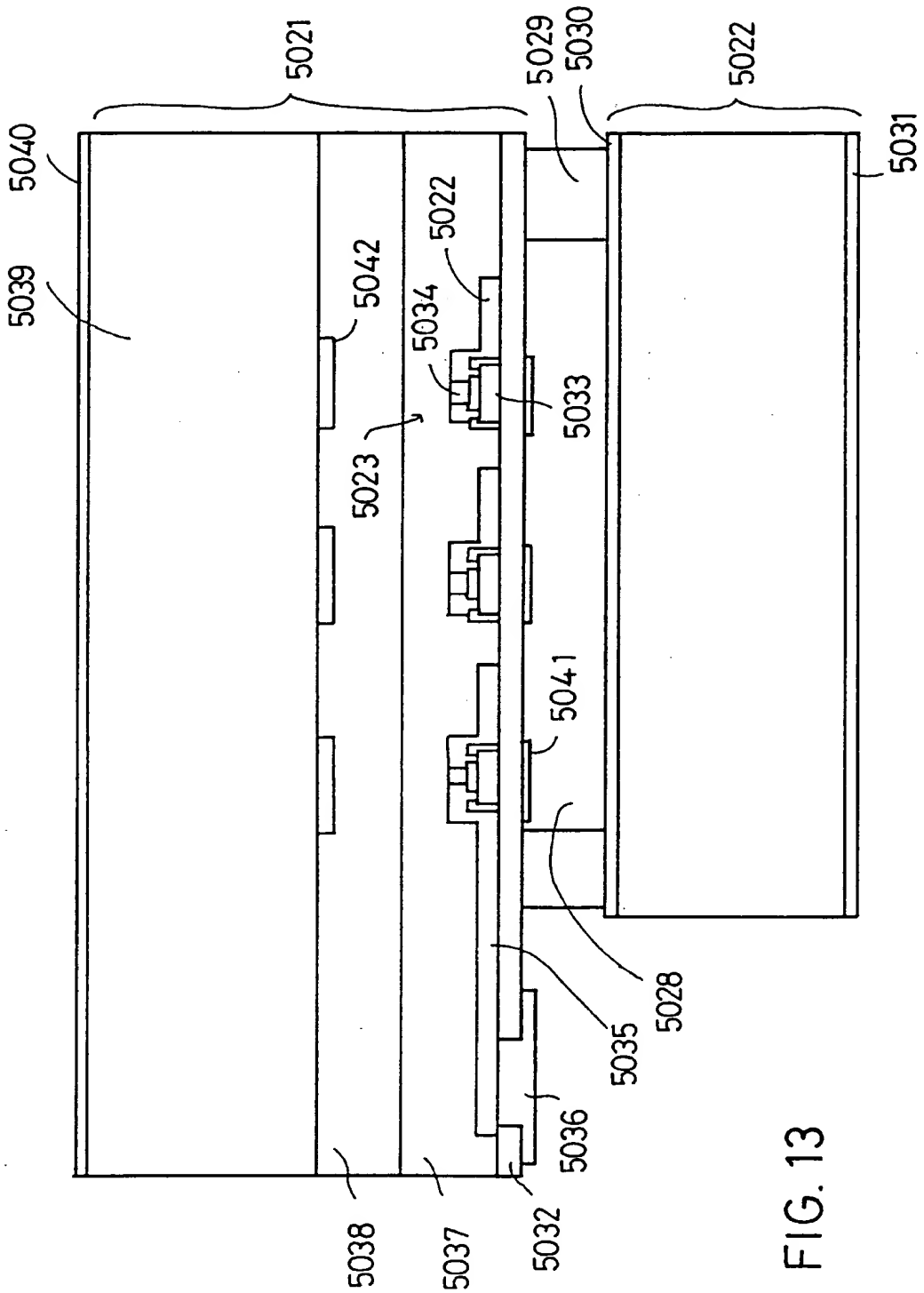

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FIG. 13

FIG. 14(A)

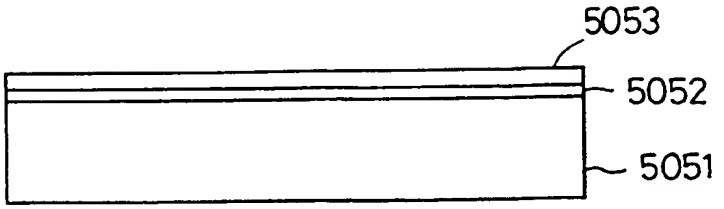


FIG. 14(B)

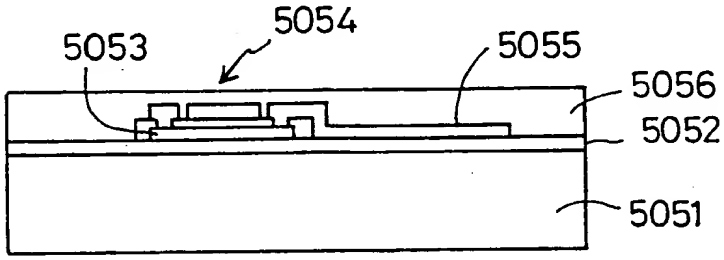


FIG. 14(C)

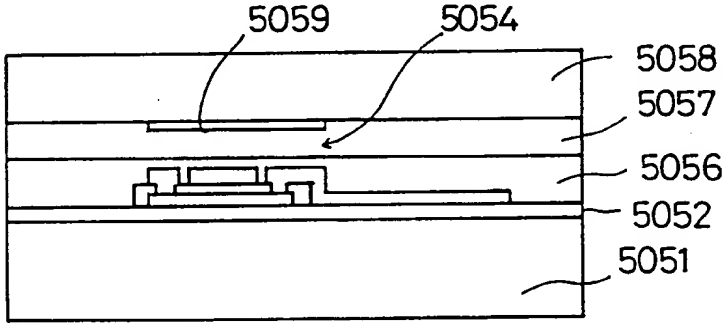


FIG. 14(D)

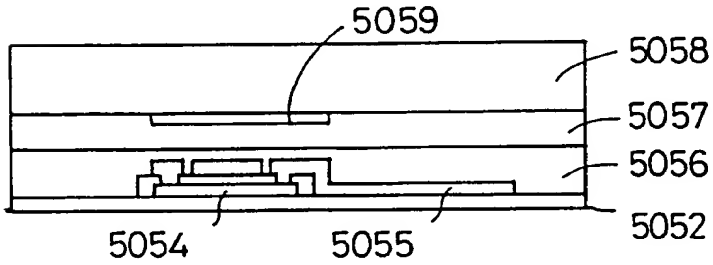


FIG. 14(E)

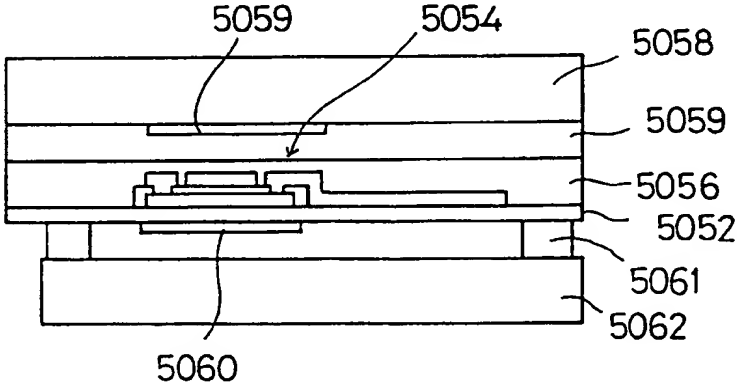
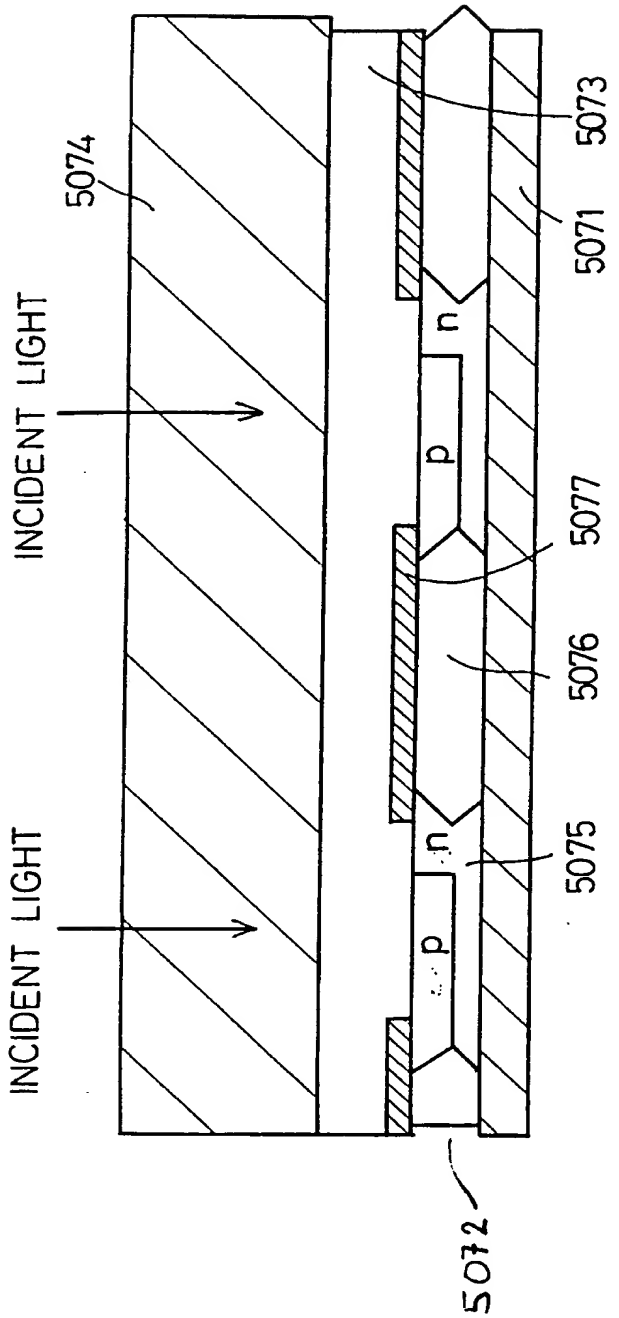


FIG. 15


INCIDENT LIGHT
INCIDENT LIGHT
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n
p
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p

FIG. 16

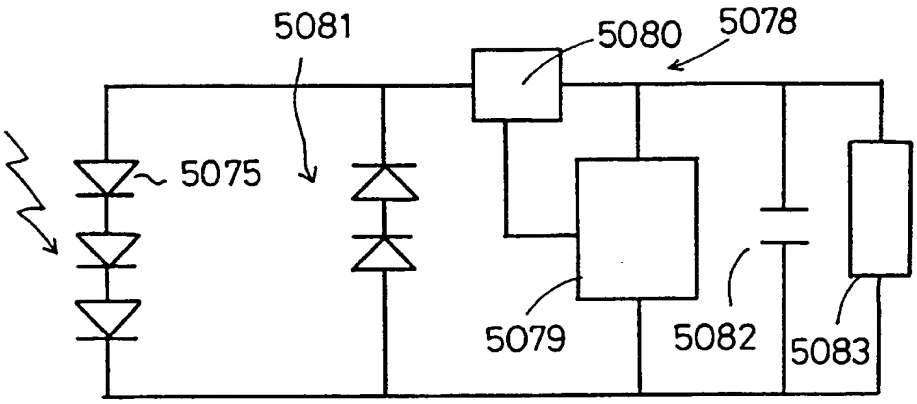

FIG. 17

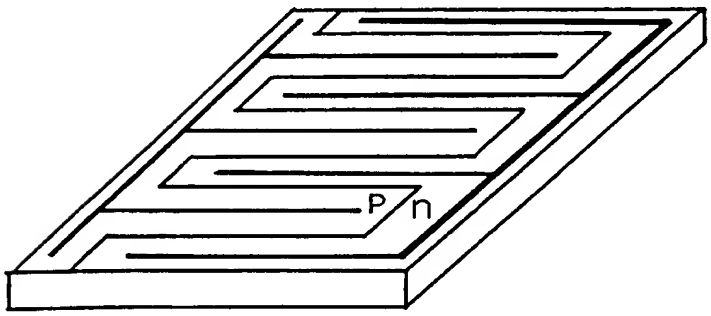

FIG. 18

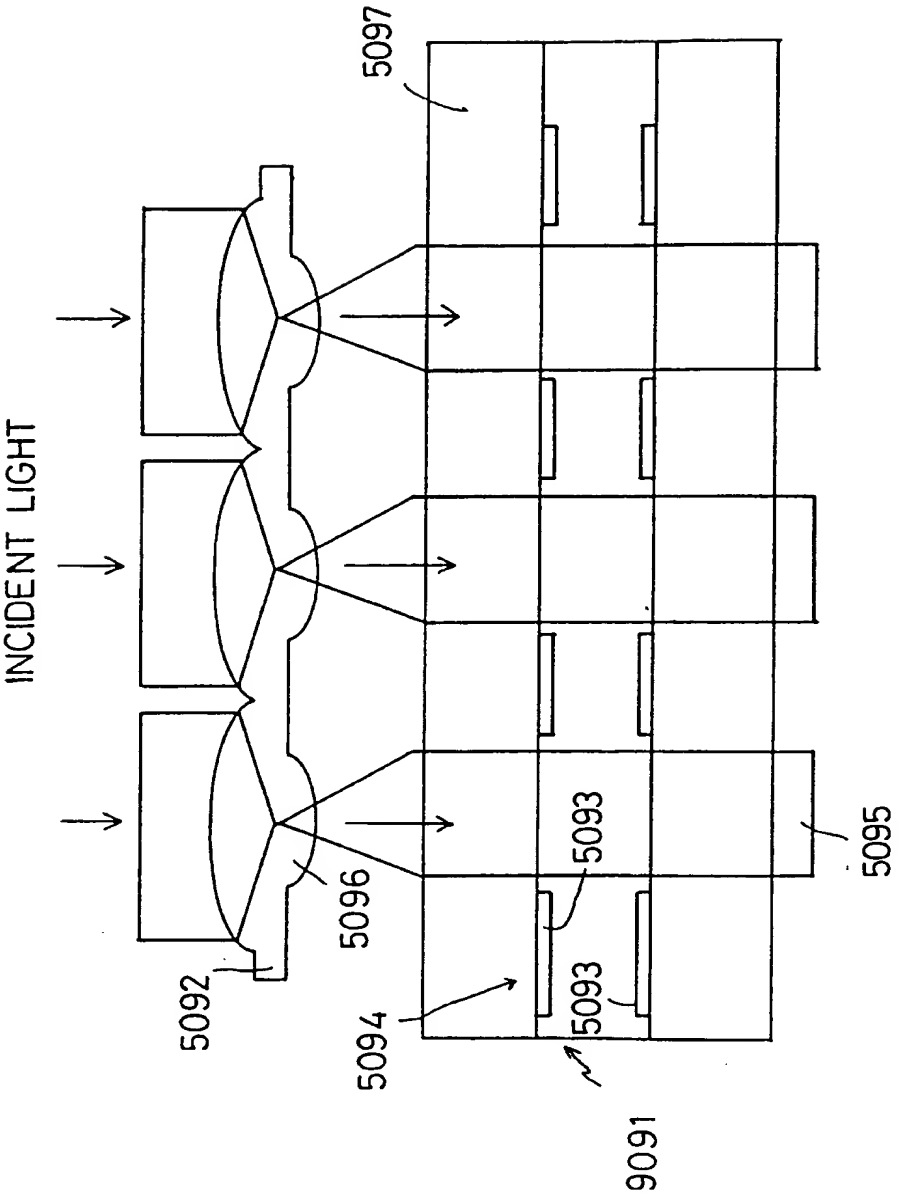

FIG. 19

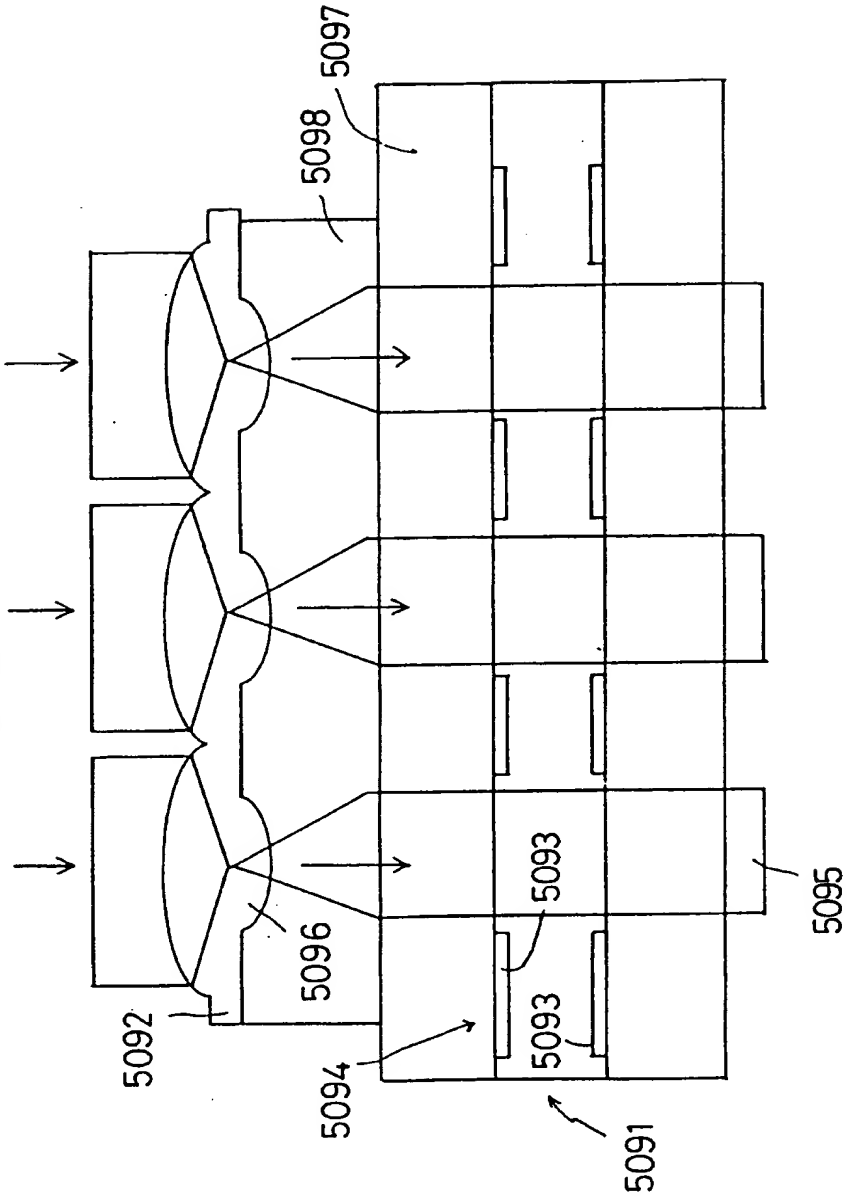

FIG. 20

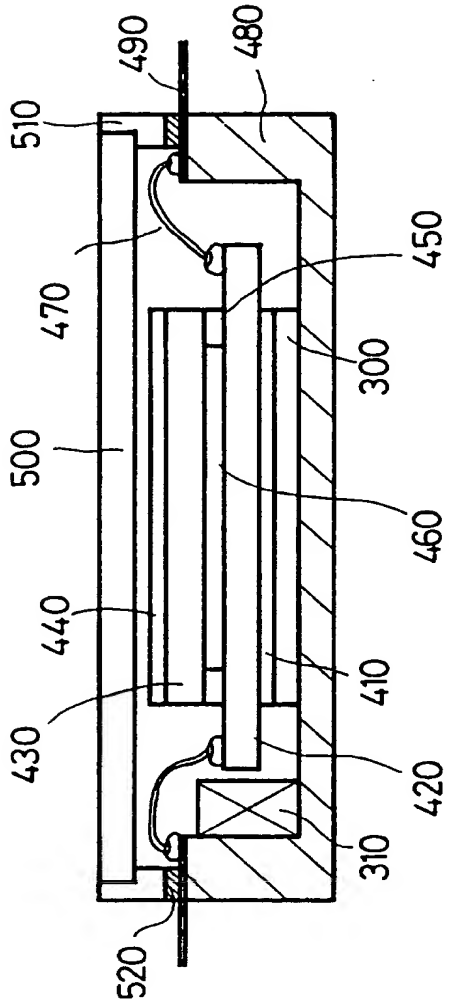

FIG. 21

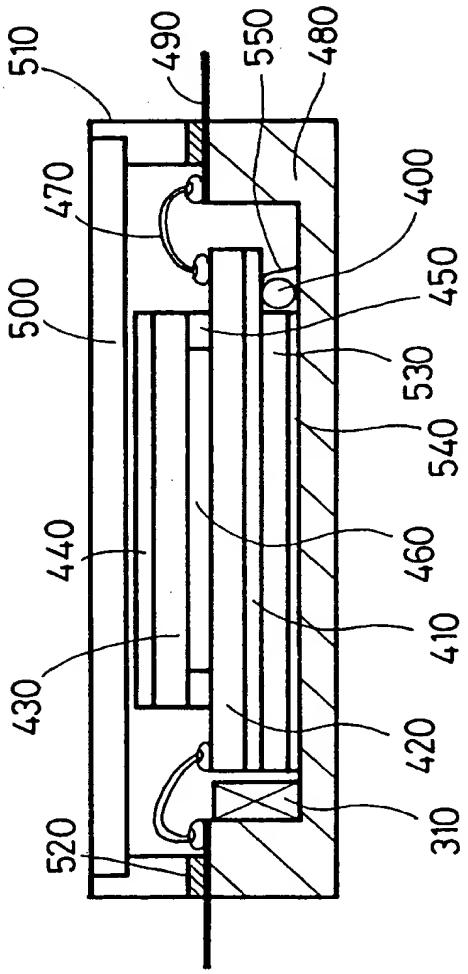
510
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FIG. 22

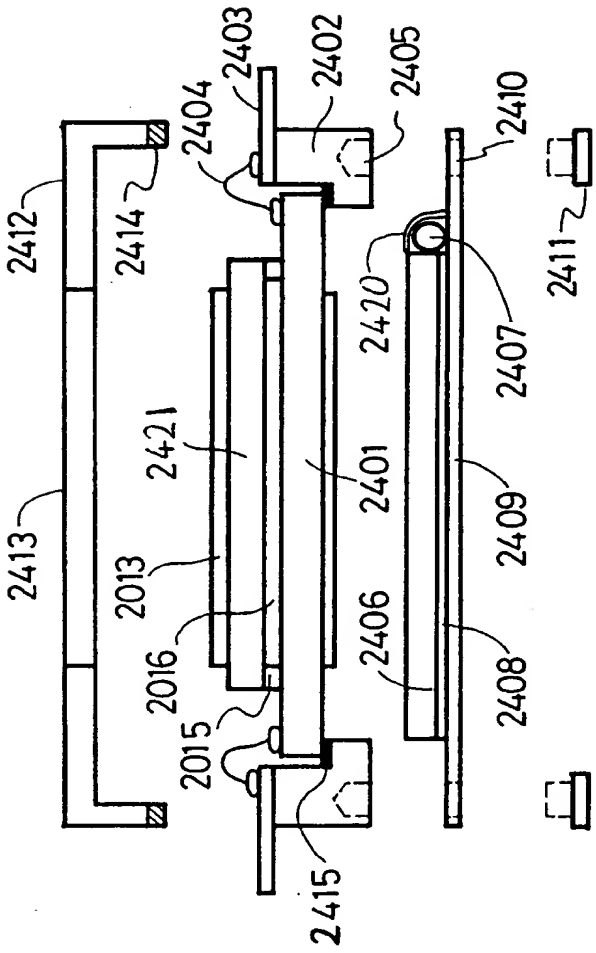
2403
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FIG. 23(A)

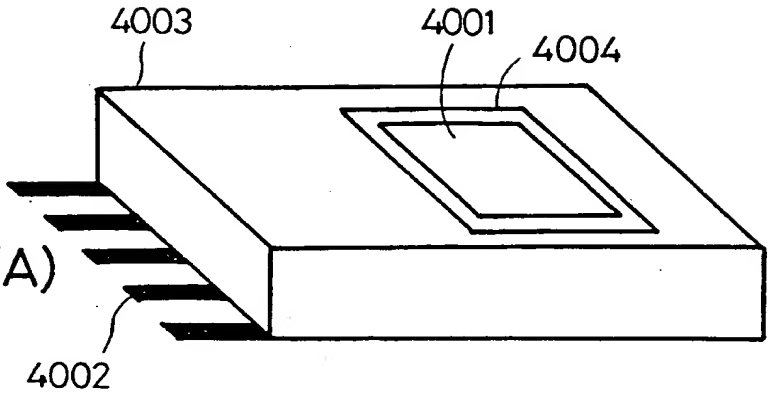

FIG. 23(B)

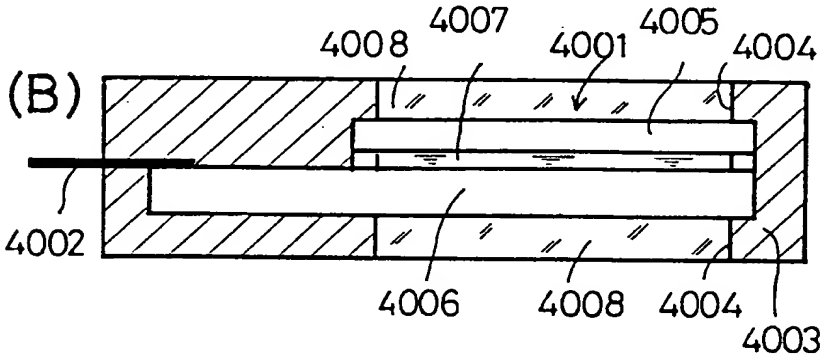

FIG. 23(C)

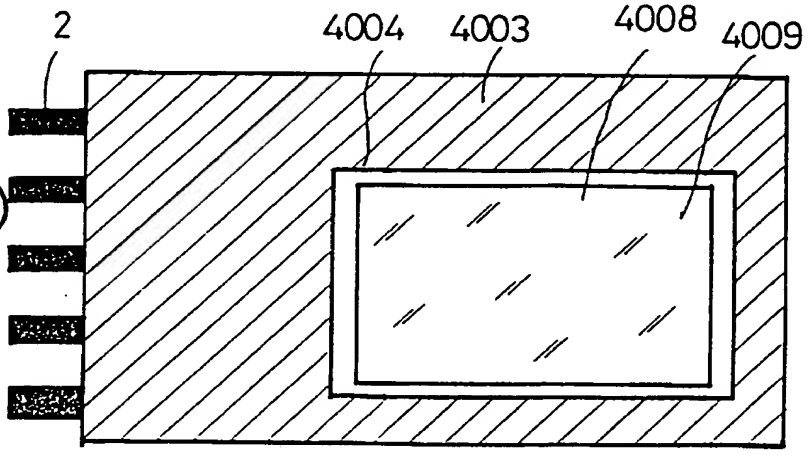

FIG. 24

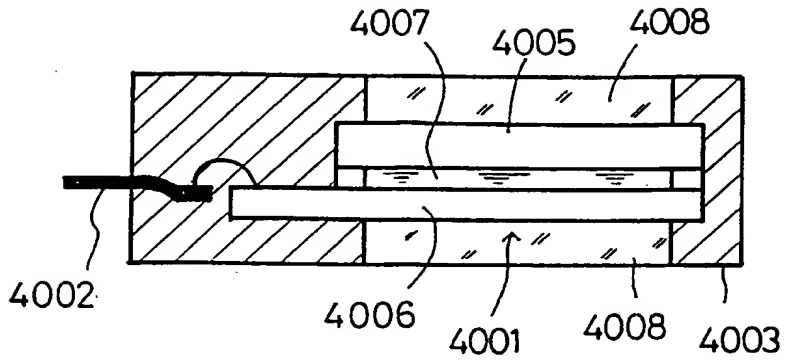

FIG. 25

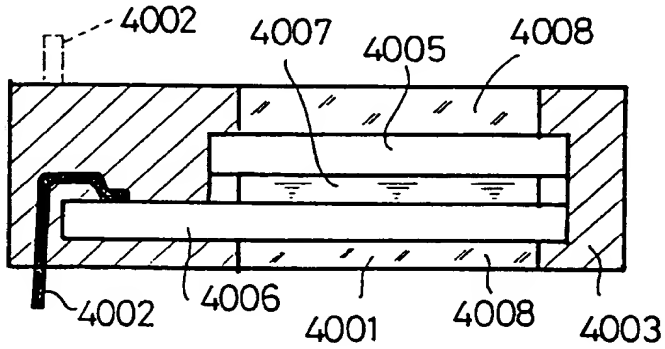

FIG. 26

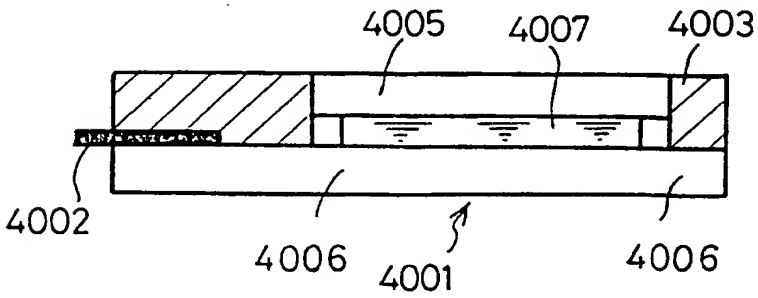

FIG. 27

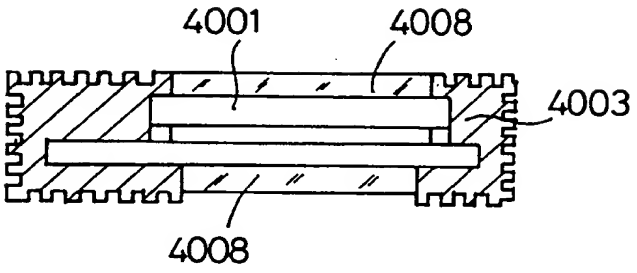

FIG. 28

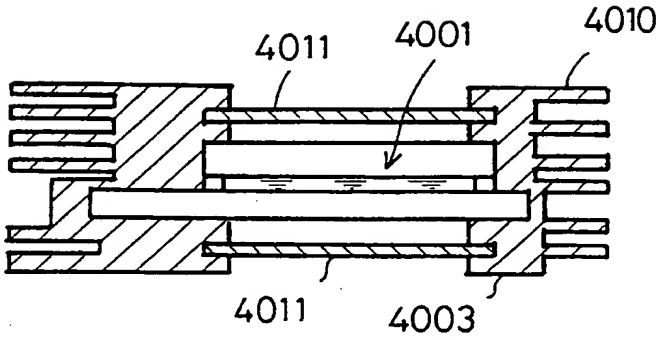

FIG. 29

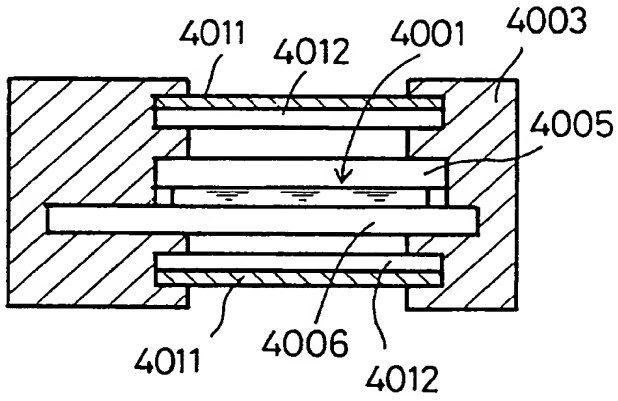

FIG. 30

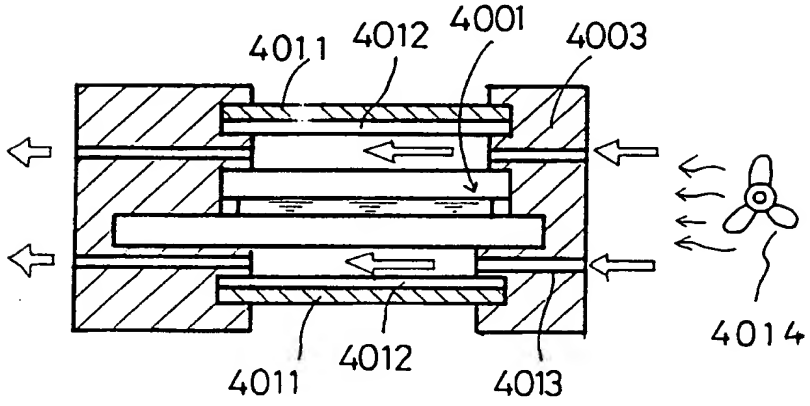

FIG. 31(A)

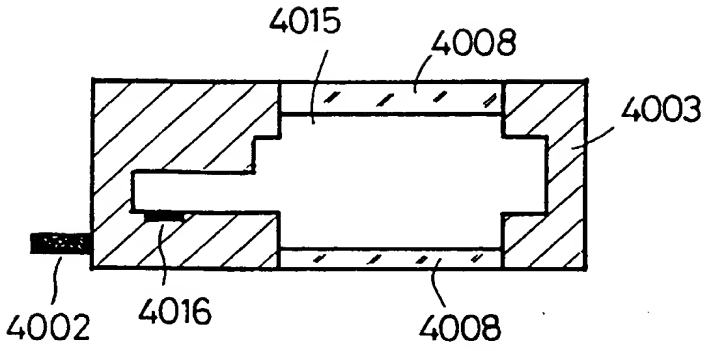

FIG. 31(B)

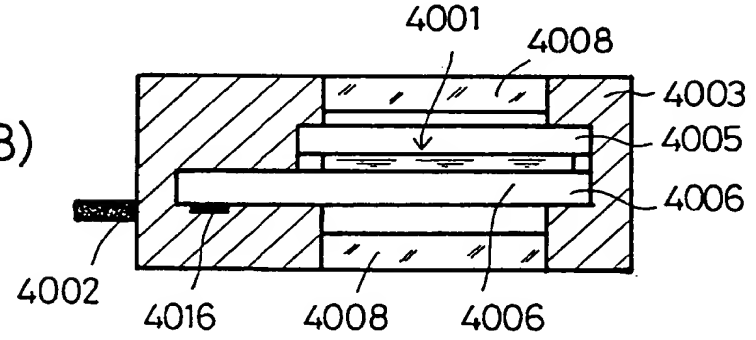

FIG. 32

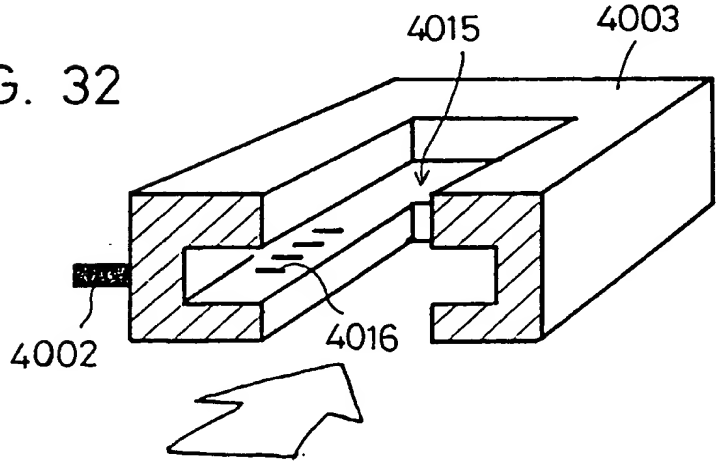

FIG. 33

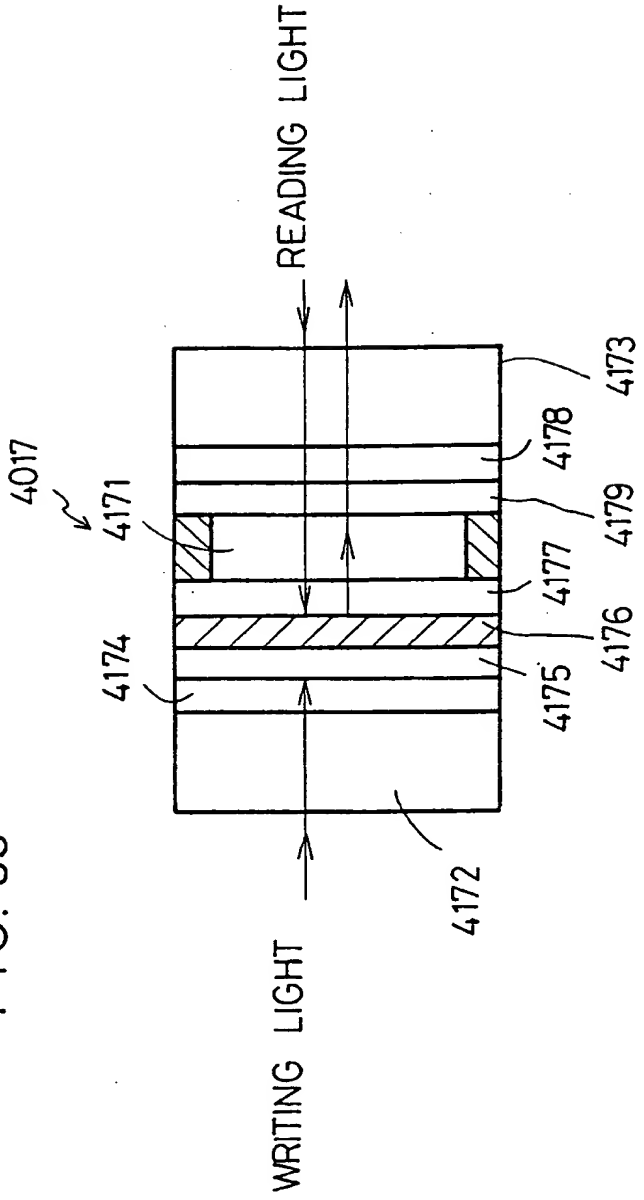
READING LIGHT
WRITING LIGHT
4017
4171
4172
4173
4174
4175
4176
4177
4178
4179

FIG. 34

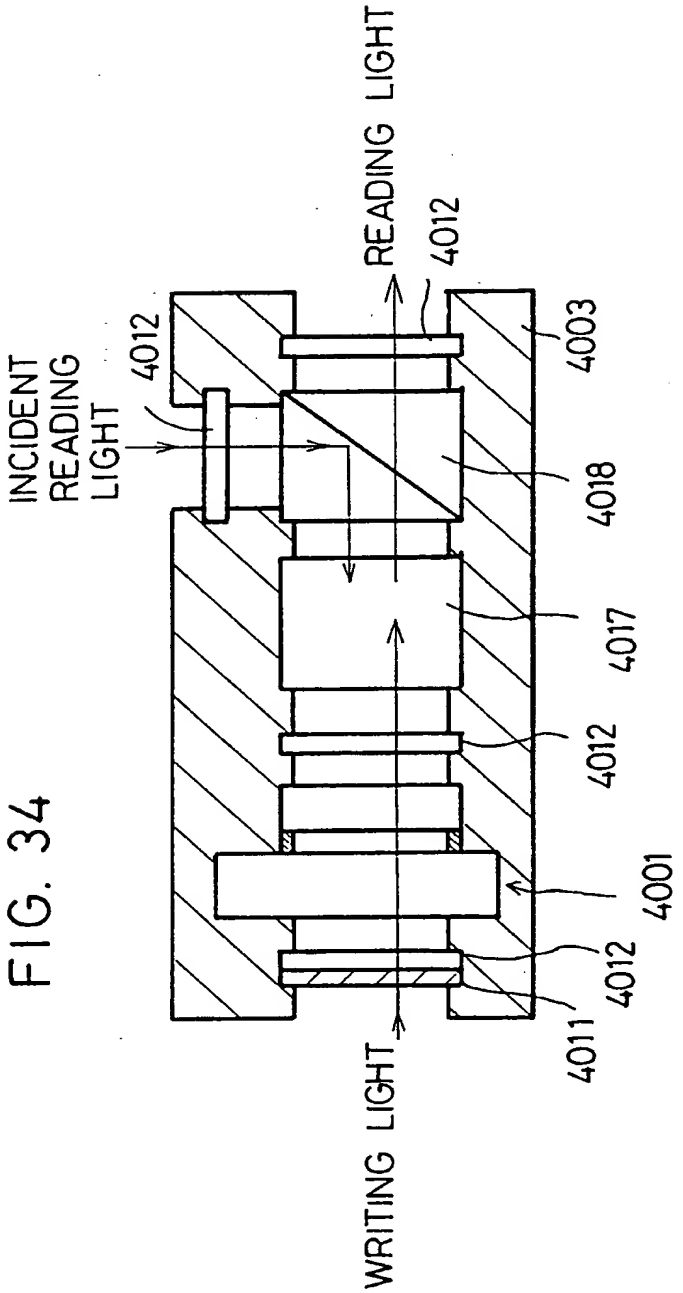
INCIDENT READING LIGHT
4012
READING LIGHT
4012
4003
4018
4017
4012
4001
4012
4011
WRITING LIGHT

FIG. 35

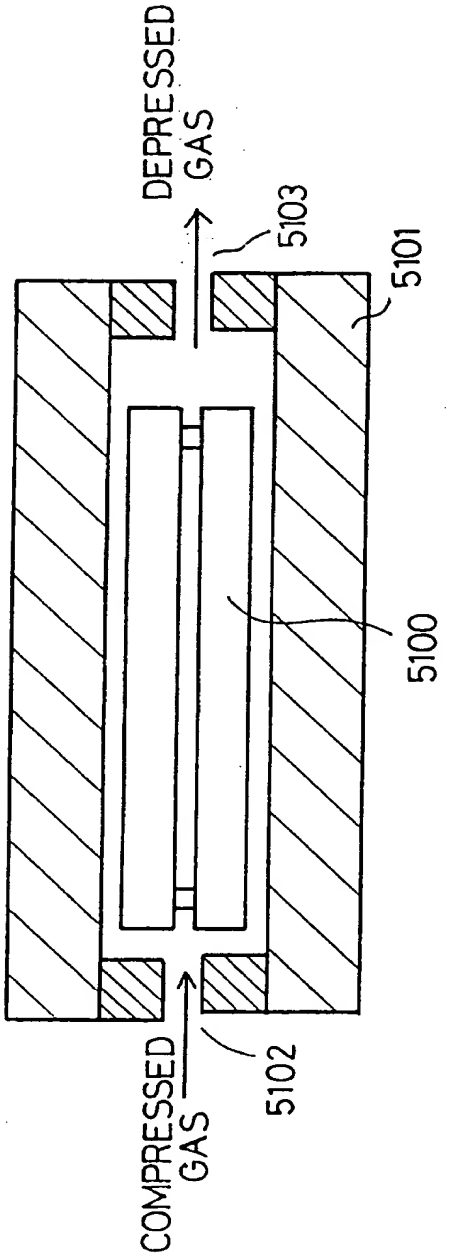

FIG. 36

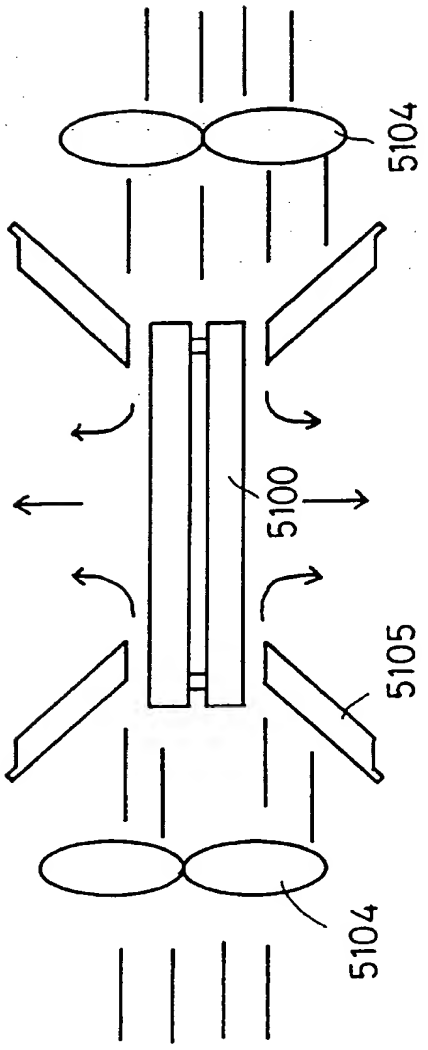

FIG. 37

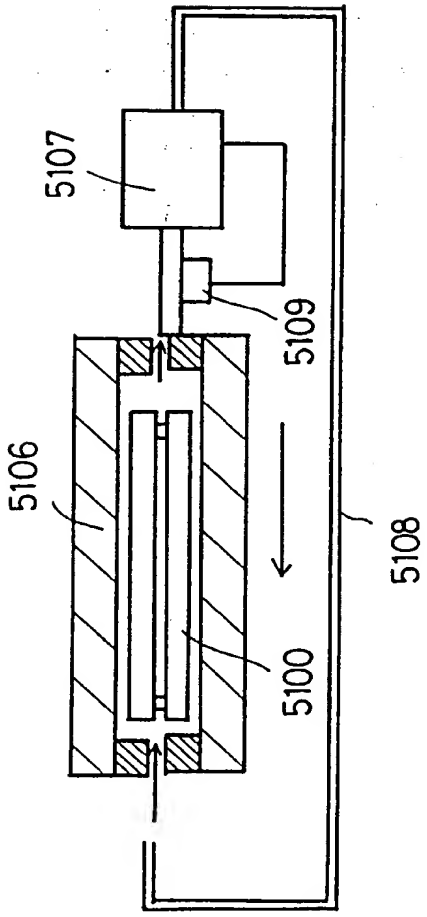

FIG. 38

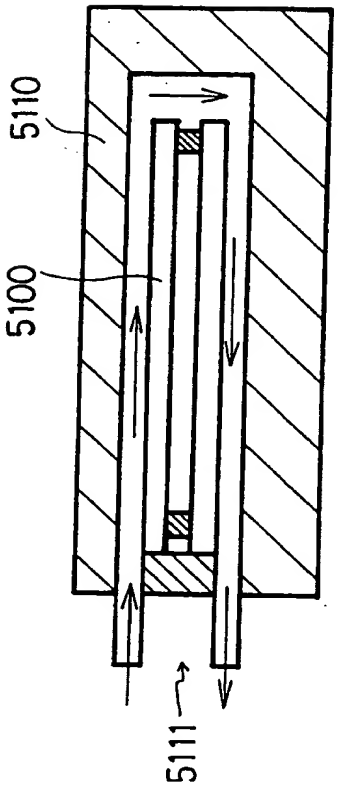

FIG. 39

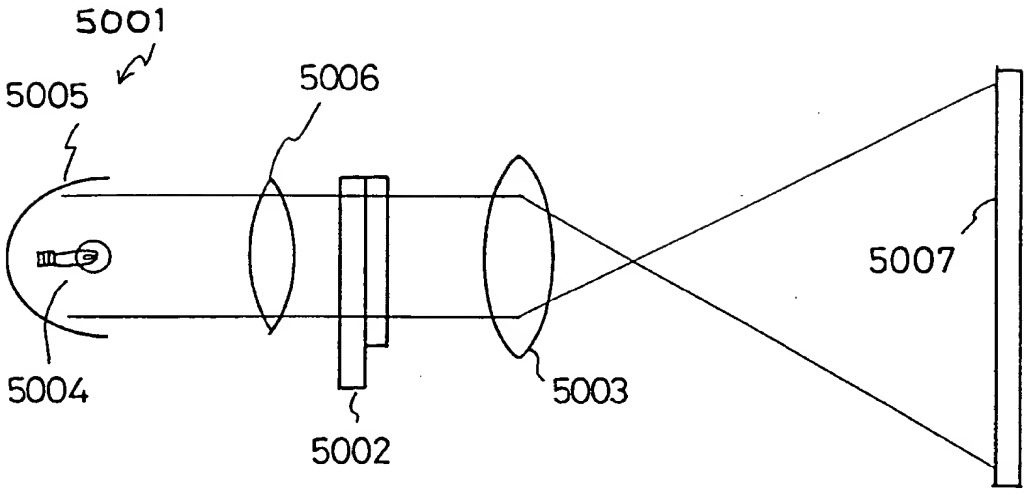

FIG. 40
PRIOR ART